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ATX
Ver: 10

CML Platform

CPU:

Comet lake S 65W

Onboard Chip

HD Audio Codec: ALC1200

LAN: Intel RTL8125B

SIO: NIC6687

Flash ROM SPI 128MB X1

System Chipset:

Z490 PCH_H

VGA Output:

HDMI Port

DP Port

Main Memory:

DDR4 (2666MHz) * 4 (Dual Channel)

PWM

IMP8-RT3609BE

ACPI

LDO

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X4) Slot * 1

PCI Express (X1) Slot * 2

M2 Slot * 2

Intel WIFI * 1

Other:

SATA30 *6

USB20 *6

REAL USB3.1 Gen2 Type A

REAL USB3.1 Gen3 Type C

REAL USB3.1 Gen1 LAN_USB

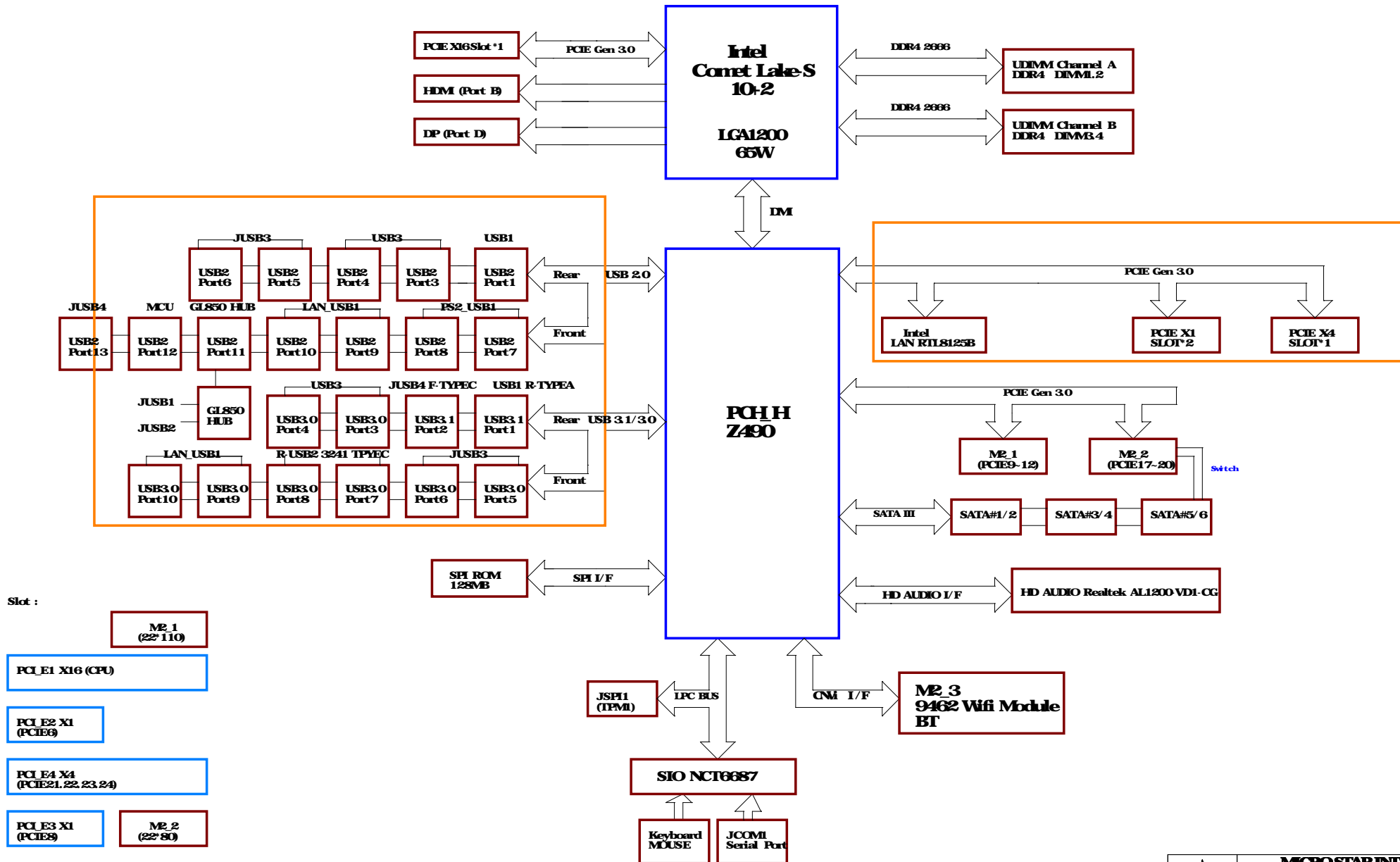
FRONT USB3.1 GEN1 TypeC

FRONT USB3.1 *2



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MS-7C79			
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MS-7C79 Block Diagram





8 M.MMA.AB6.Q

CPU1A

CML5

M.MMA.A0	AV18	DORO.MA[0]
M.MMA.A1	AV25	DORO.MA[1]
M.MMA.A2	AV24	DORO.MA[2]
M.MMA.A3	AV25	DORO.MA[3]
M.MMA.A4	AV25	DORO.MA[4]
M.MMA.A5	AV25	DORO.MA[5]
M.MMA.A6	AV25	DORO.MA[6]
M.MMA.A7	AV27	DORO.MA[7]
M.MMA.A8	AV27	DORO.MA[8]
M.MMA.A9	AV28	DORO.MA[9]
M.MMA.A10	AV17	DORO.MA[10]
M.MMA.A11	AV27	DORO.MA[11]
M.MMA.A12	AV28	DORO.MA[12]
M.MMA.A13	AV14	DORO.MA[13]
M.MMA.A14	AV16	DORO.MA[14]
M.MMA.A15	AV16	DORO.MA[15]
M.MMA.A16	AV16	DORO.MA[16]

8 M.MMA.A16.Q

MACT.A.N

AV30

DORO.ACT#

8 M.CRE.A0

M.CRE.A0

AV31

DORO.CRE[0]

8 M.CRE.A1

M.CRE.A1

AV31

DORO.CRE[1]

8 M.CRE.A2

M.CRE.A2

AV31

DORO.CRE[2]

8 M.CRE.A3

M.CRE.A3

AV31

DORO.CRE[3]

8 M.CS#A0

M.CS#A0

AV15

DORO.CS#0

8 M.CS#A1

M.CS#A1

AV15

DORO.CS#1

8 M.CS#A2

M.CS#A2

AV15

DORO.CS#2

8 M.CS#A3

M.CS#A3

AV15

DORO.CS#3

8 M.CDI.A0

M.CDI.A0

AV14

DORO.CDI[0]

8 M.CDI.A1

M.CDI.A1

AV14

DORO.CDI[1]

8 M.CDI.A2

M.CDI.A2

AV14

DORO.CDI[2]

8 M.CDI.A3

M.CDI.A3

AV14

DORO.CDI[3]

8 M.BA.A.0

M.BA.A.0

AV16

DORO.BA[0]

8 M.BA.A.1

M.BA.A.1

AV17

DORO.BA[1]

8 M.BG.A.0

M.BG.A.0

AV29

DORO.BG[0]

8 M.BG.A.1

M.BG.A.1

AV29

DORO.BG[1]

8 M.CKA.DFO

M.CKA.DFO

AV24

DORO.CKA[0]

8 M.CKA.DN0

M.CKA.DN0

AV24

DORO.CKA[0]

8 M.CKA.DN1

M.CKA.DN1

AV23

DORO.CKA[1]

8 M.CKA.DN2

M.CKA.DN2

AV23

DORO.CKA[2]

8 M.CKA.DN3

M.CKA.DN3

AV23

DORO.CKA[3]

8 M.CKA.DN4

M.CKA.DN4

AV23

DORO.CKA[4]

8 M.CKA.DN5

M.CKA.DN5

AV23

DORO.CKA[5]

8 M.CKA.DN6

M.CKA.DN6

AV23

DORO.CKA[6]

8 M.CKA.DN7

M.CKA.DN7

AV23

DORO.CKA[7]

8 M.CKA.DN8

M.CKA.DN8

AV23

DORO.CKA[8]

8 M.CKA.DN9

M.CKA.DN9

AV23

DORO.CKA[9]

8 M.CKA.DN10

M.CKA.DN10

AV23

DORO.CKA[10]

8 M.CKA.DN11

M.CKA.DN11

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DORO.CKA[11]

8 M.CKA.DN12

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DORO.CKA[12]

8 M.CKA.DN13

M.CKA.DN13

AV23

DORO.CKA[13]

8 M.CKA.DN14

M.CKA.DN14

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DORO.CKA[14]

8 M.CKA.DN15

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AV23

DORO.CKA[15]

8 M.CKA.DN16

M.CKA.DN16

AV23

DORO.CKA[16]

8 M.CKA.DN17

M.CKA.DN17

AV23

DORO.CKA[17]

8 M.CKA.DN18

M.CKA.DN18

AV23

DORO.CKA[18]

8 M.CKA.DN19

M.CKA.DN19

AV23

DORO.CKA[19]

8 M.CKA.DN20

M.CKA.DN20

AV23

DORO.CKA[20]

8 M.CKA.DN21

M.CKA.DN21

AV23

DORO.CKA[21]

8 M.CKA.DN22

M.CKA.DN22

AV23

DORO.CKA[22]

AE39 M.DATA.A4

AE38 M.DATA.A5

AE38 M.DATA.A7

AE38 M.DATA.A5

AE40 M.DATA.A7

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AE40 M.DATA.A5

M.DATA.AB6.Q 8

9 M.MMA.AB6.Q

CPU1B

CML5

M.MMA.B0	AP19	DORO.MA[0]
M.MMA.B1	AP20	DORO.MA[1]
M.MMA.B2	AP20	DORO.MA[2]
M.MMA.B3	AP21	DORO.MA[3]
M.MMA.B4	AP21	DORO.MA[4]
M.MMA.B5	AP21	DORO.MA[5]
M.MMA.B6	AP22	DORO.MA[6]
M.MMA.B7	AP21	DORO.MA[7]
M.MMA.B8	AP22	DORO.MA[8]
M.MMA.B9	AP23	DORO.MA[9]
M.MMA.B10	AP23	DORO.MA[10]
M.MMA.B11	AP23	DORO.MA[11]
M.MMA.B12	AP24	DORO.MA[12]
M.MMA.B13	AP25	DORO.MA[13]
M.MMA.B14	AP25	DORO.MA[14]
M.MMA.B15	AP26	DORO.MA[15]
M.MMA.B16	AP26	DORO.MA[16]

9 M.MMA.AB6.Q

MACT.B.N

AP25

DORO.ACT#

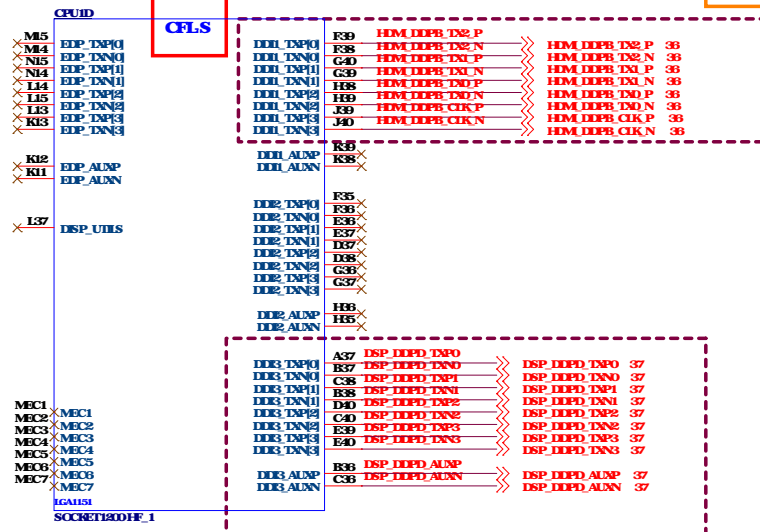
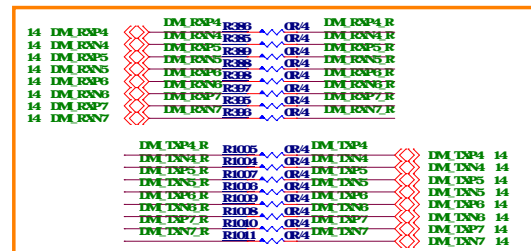
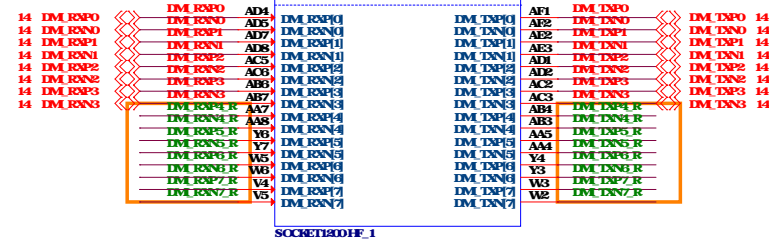
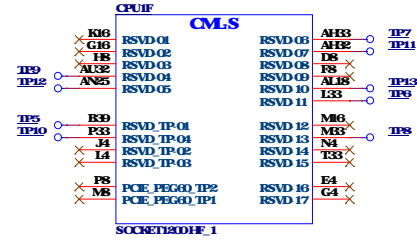
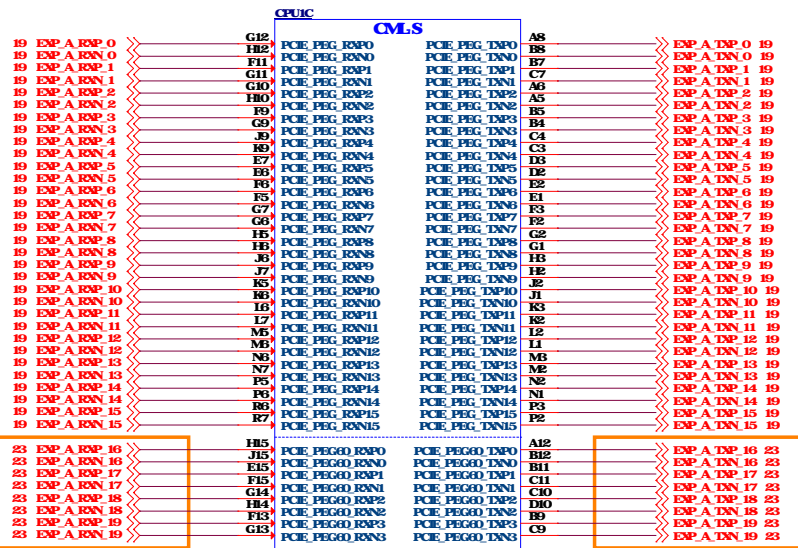
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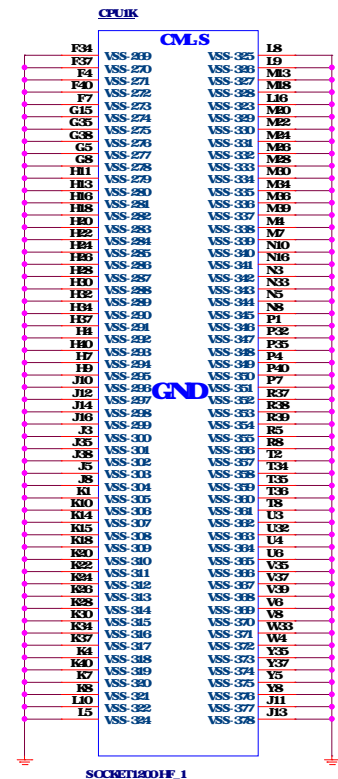
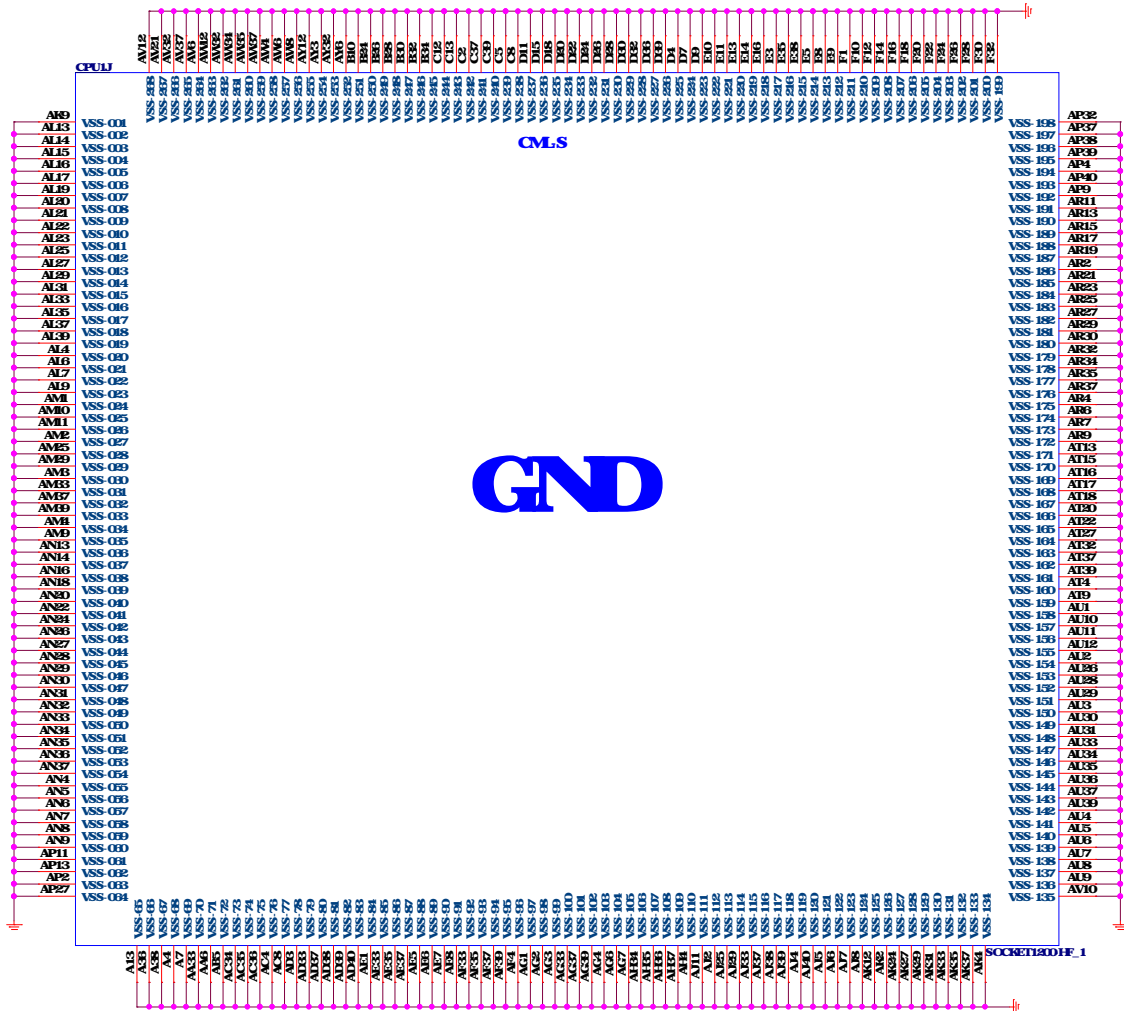
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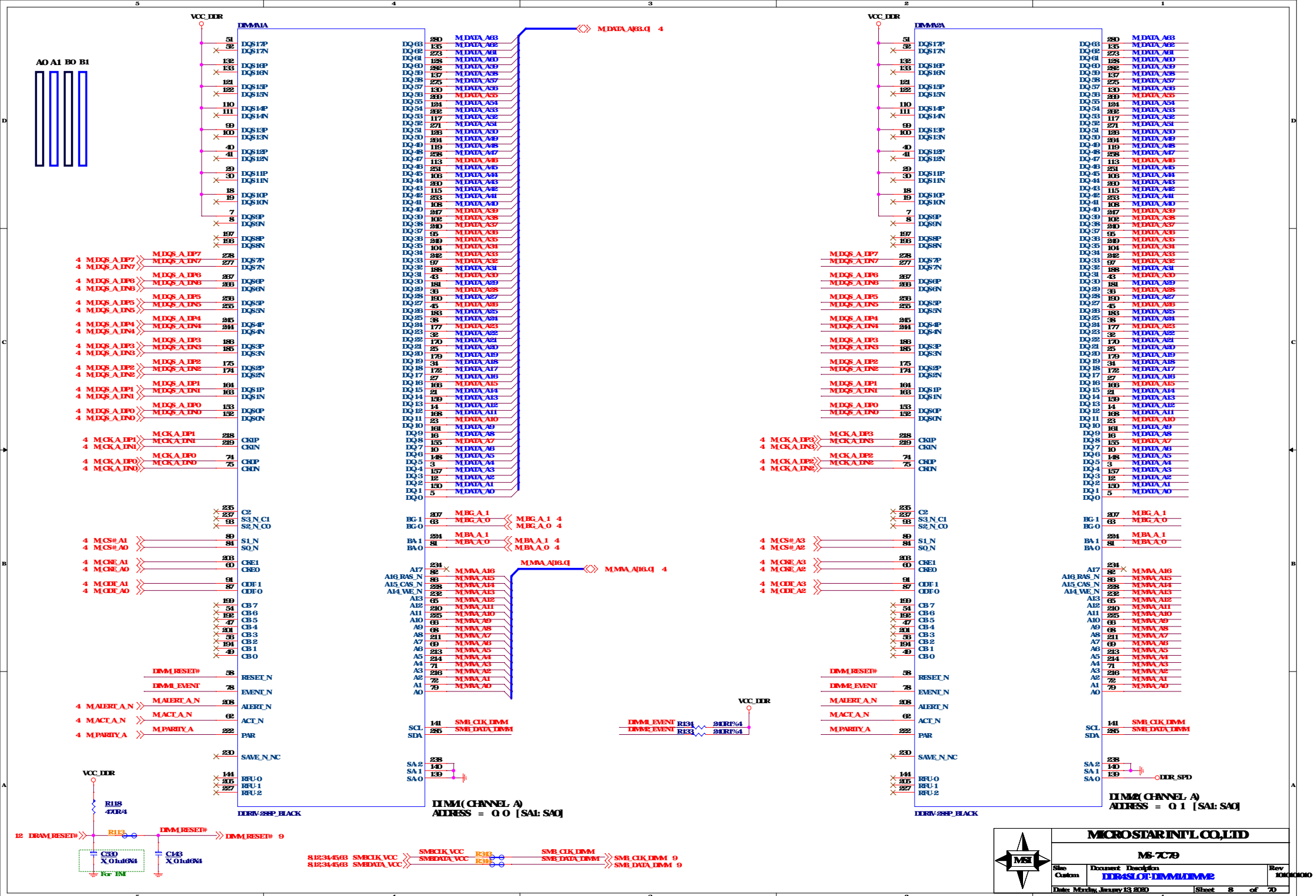
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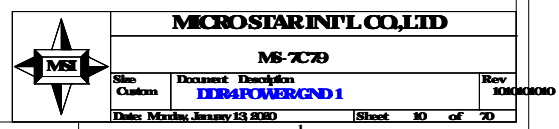
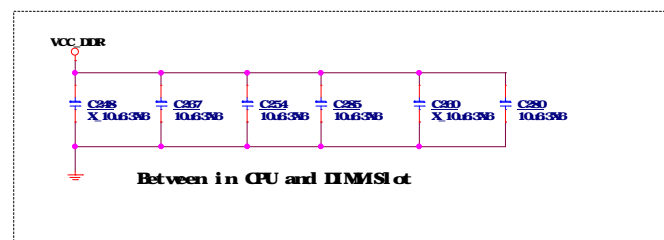
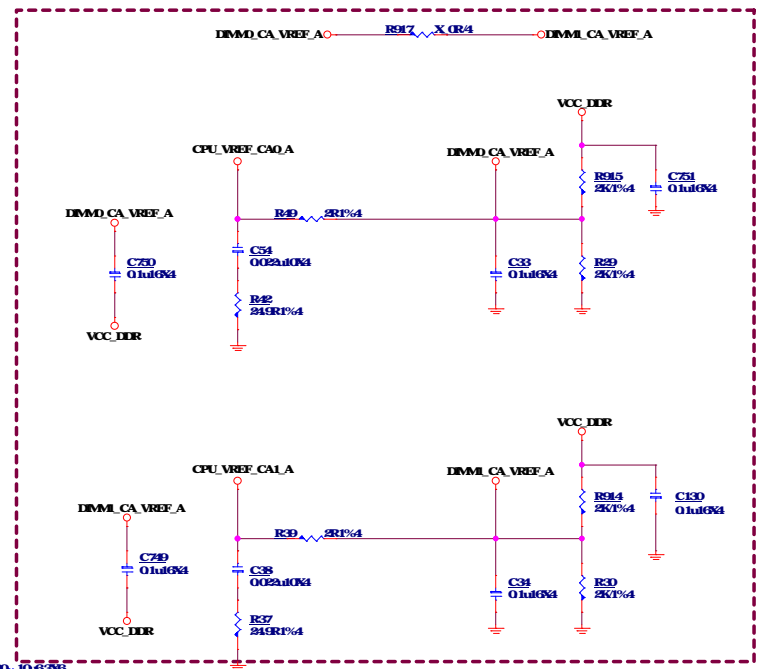
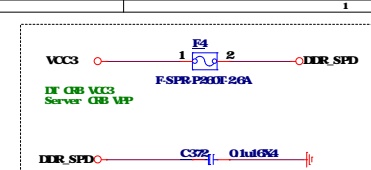
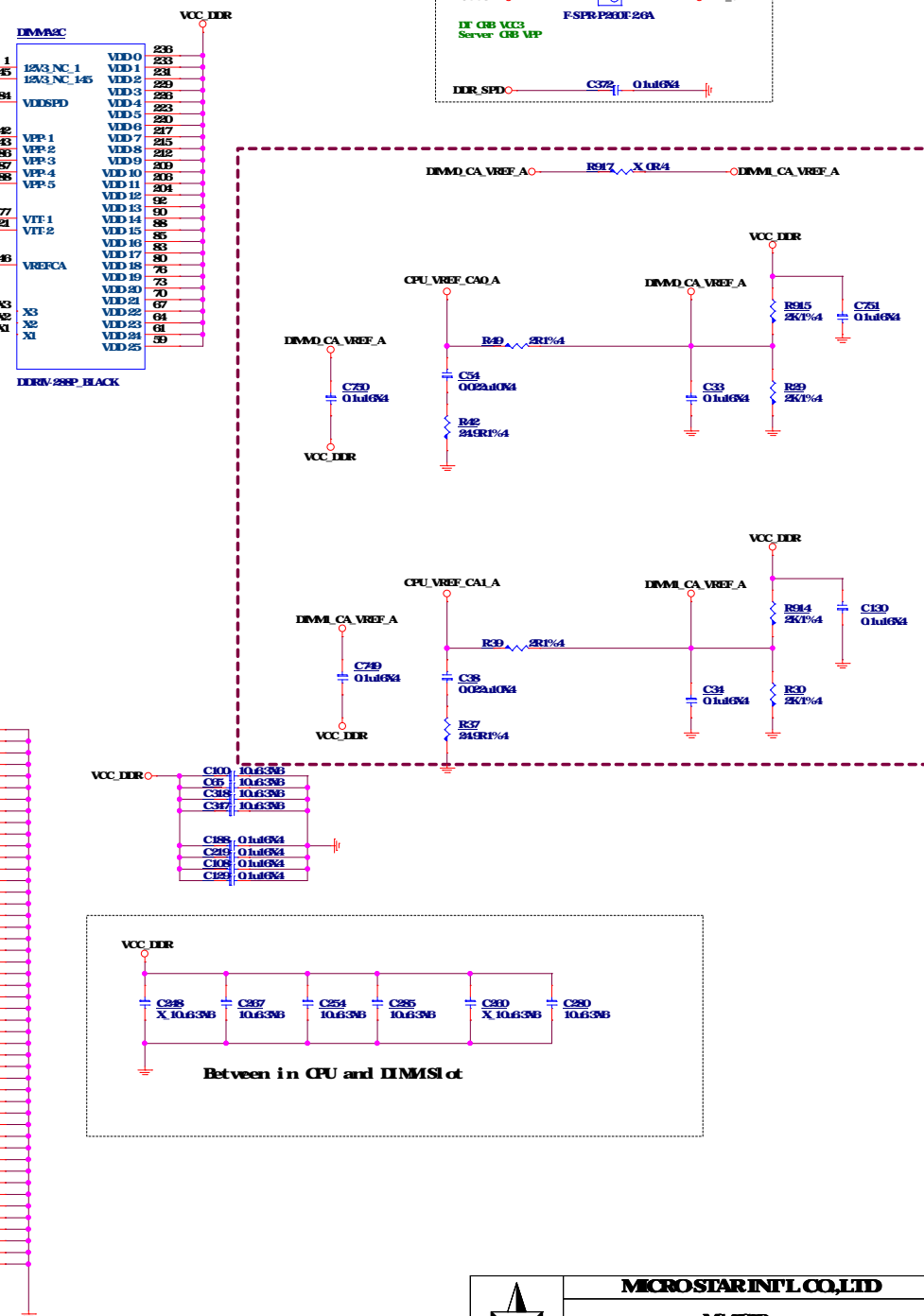
DORO.CRE[0]

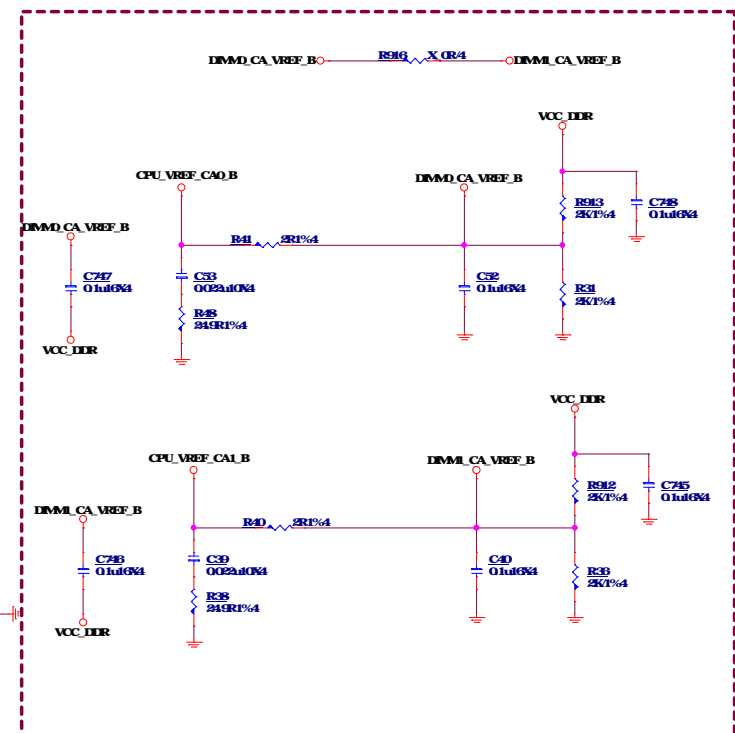
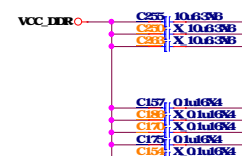
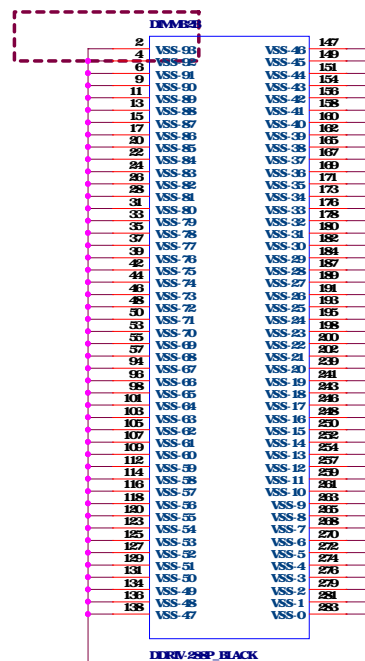
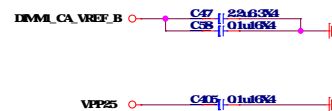
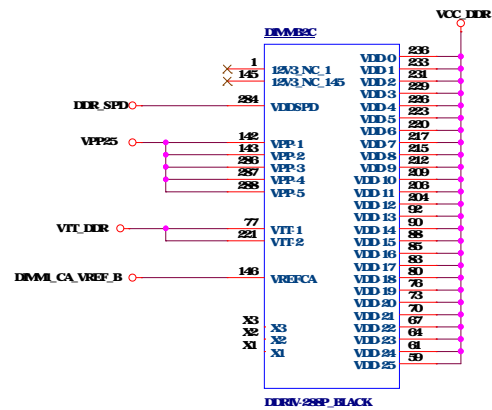
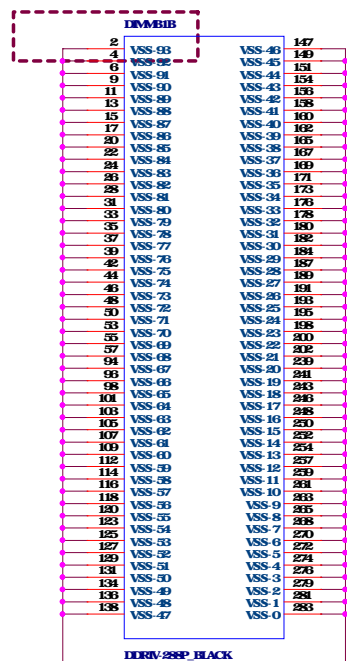
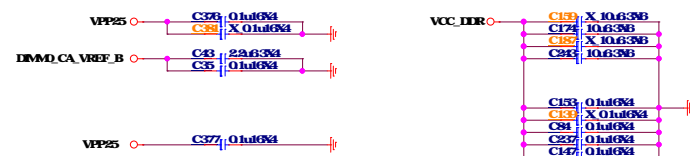
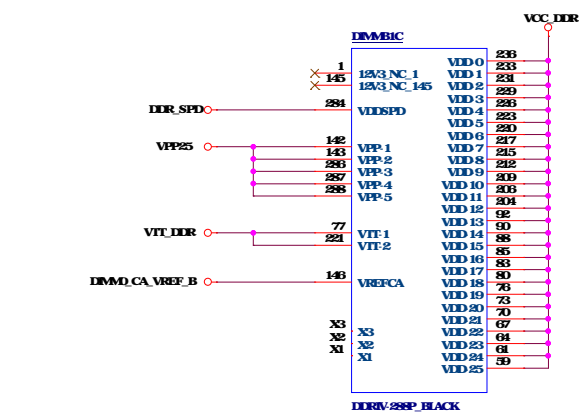
9 M.CRE.B1









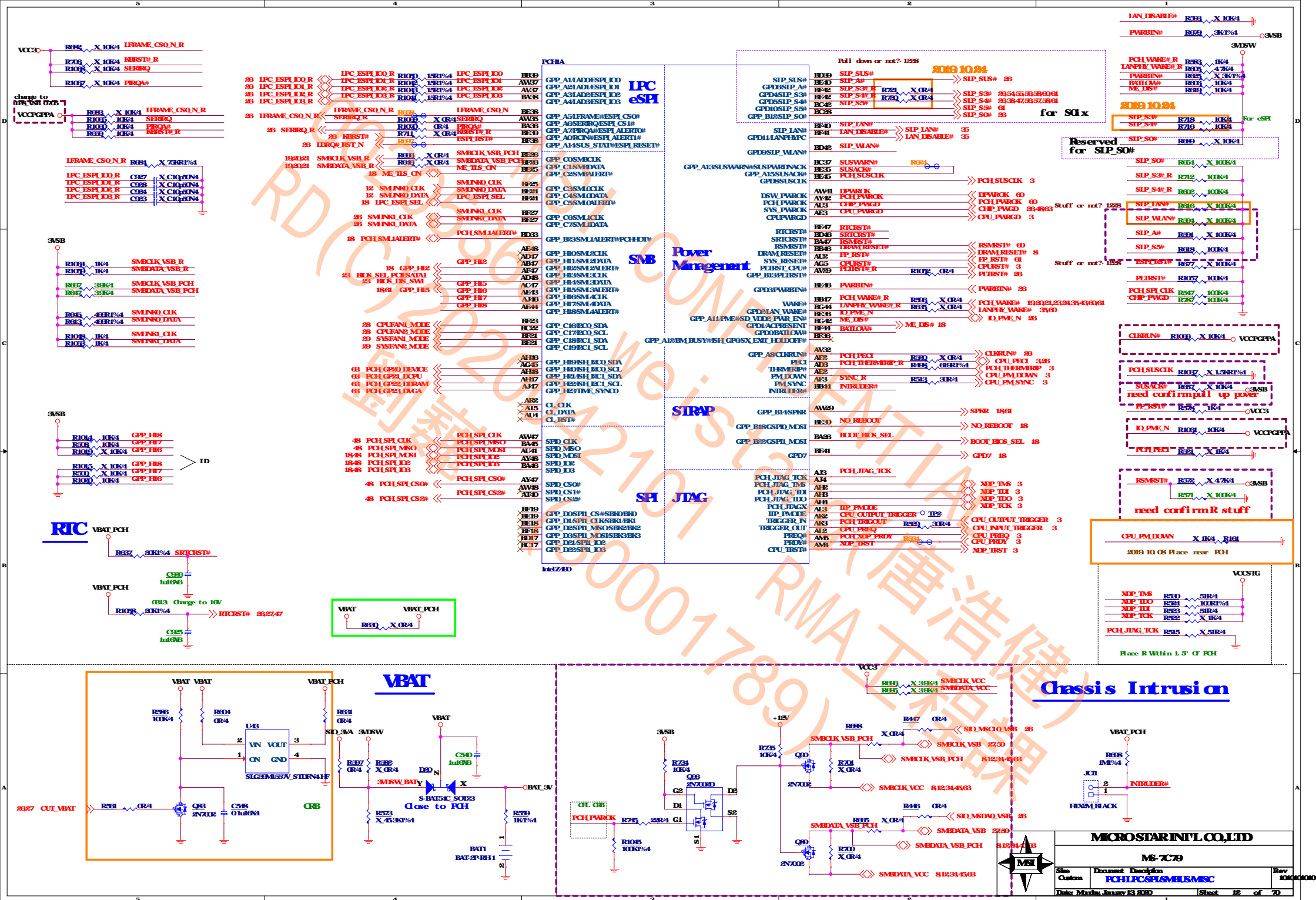


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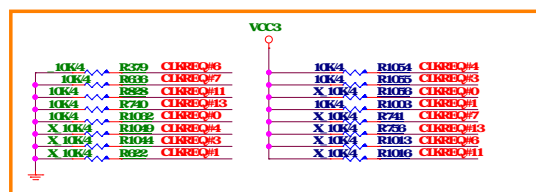
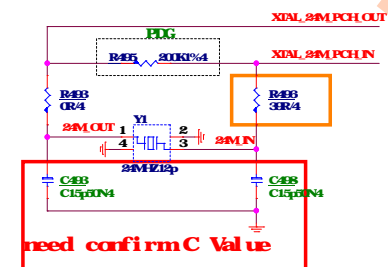
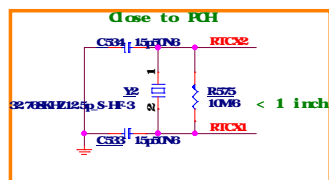
MS-7C79

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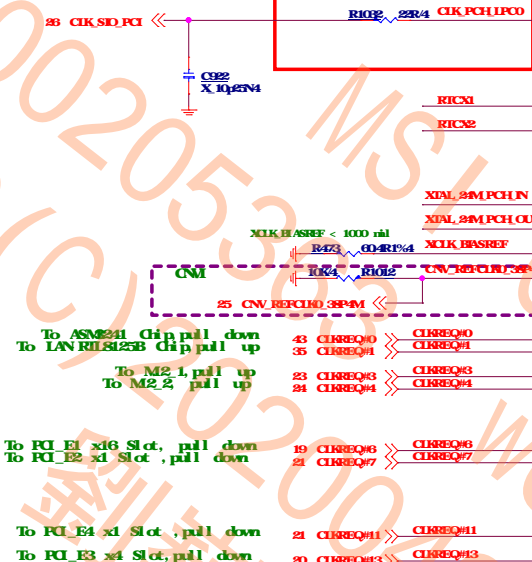
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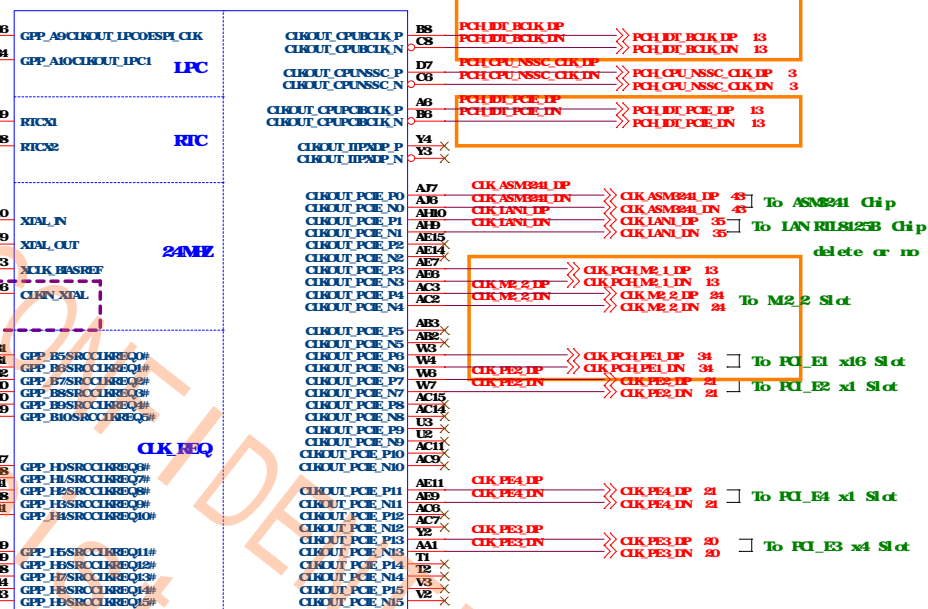
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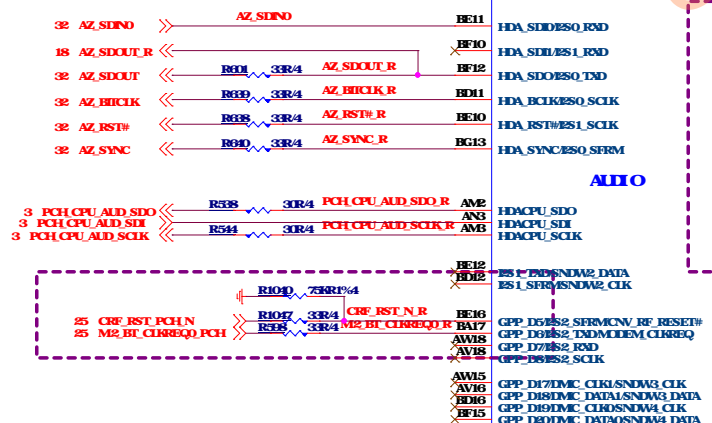


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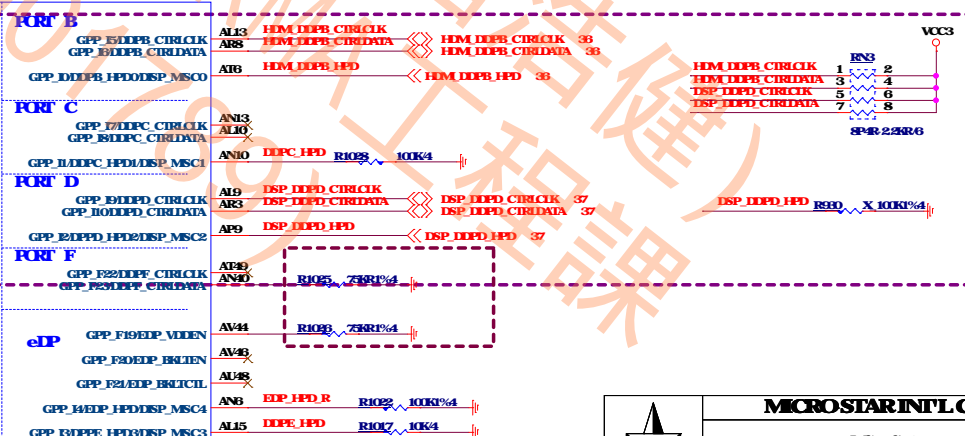
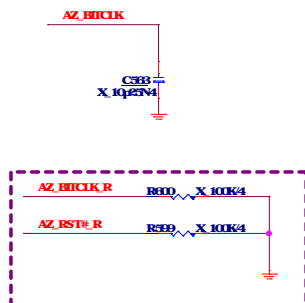


Intel Z490

PC-HID



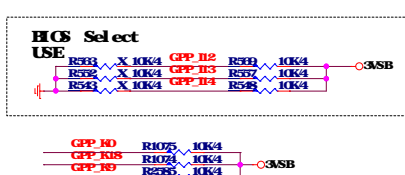
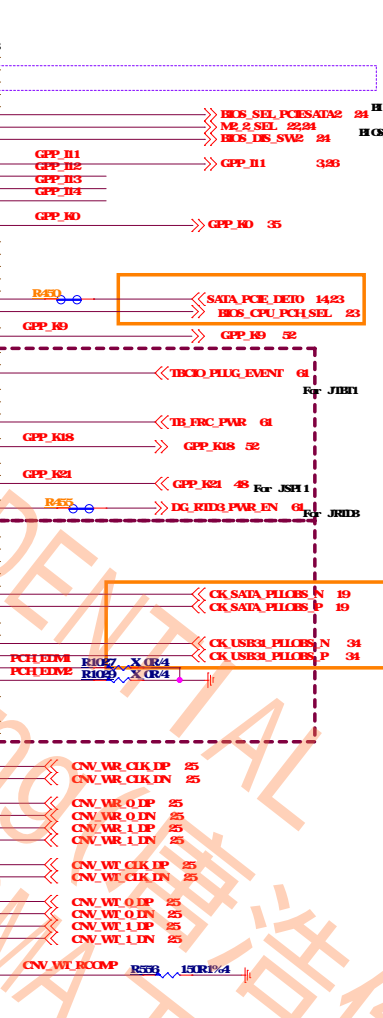
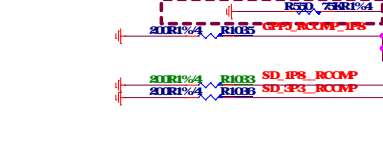
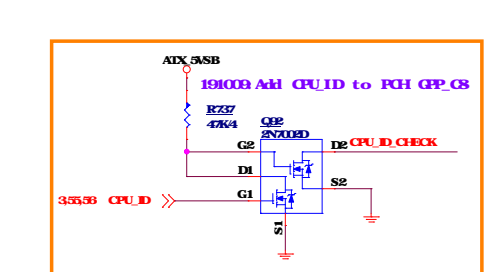
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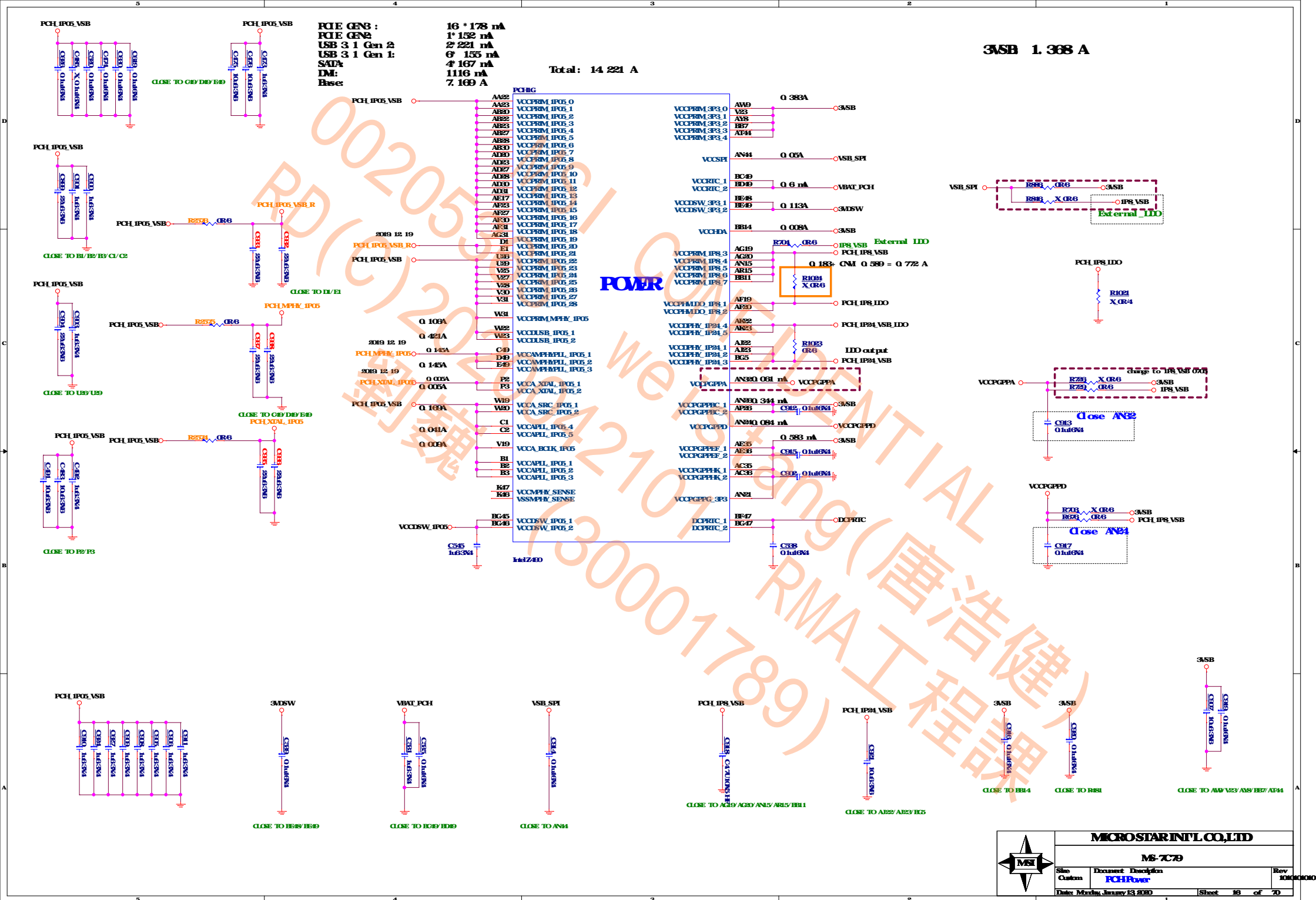


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Date: Monday, January 13, 2020		Sheet 13 of 20





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VSS



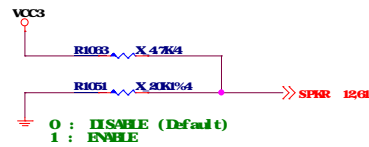
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MS-7C79

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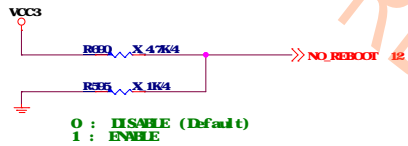
Date: Monday, January 13, 2003 Sheet: 17 of 20

TCP Swap



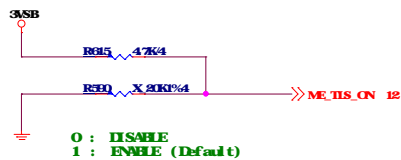
Internal Pull-down is disabled after PCHPMCK is High

No Reboot



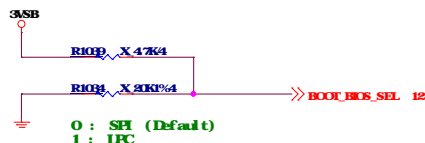
Internal Pull-down is disabled after PCHPMCK is High

TLS confidentiality



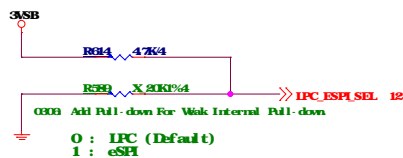
Internal Pull-down is disabled after RSMST# de-assert.

Boot HCS



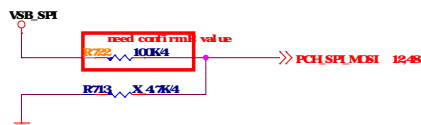
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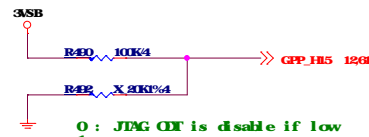


Internal Pull-down is disabled after RSMST# de-assert.

Reserved

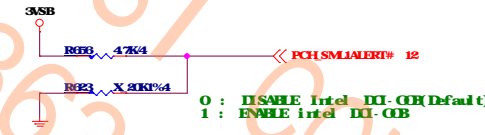


OT Disable



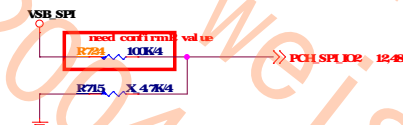
Internal Pull-down is disabled after RSMST# de-assert.

DDI Enable

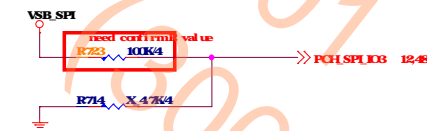


Internal Pull-down is disabled after RSMST# de-assert.

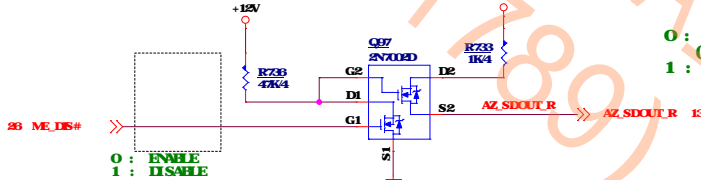
Reserved



Reserved



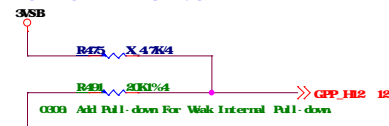
Flash Descriptor Security Override



0 : Enable security measures defined in the Flash Descriptor. (Default)
1 : DISABLE Flash Descriptor Security(Override).

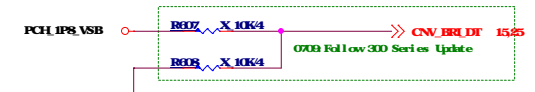
Internal Pull-down is disabled after PCHPMCK is High

ESPI FLASH SHARING MODE



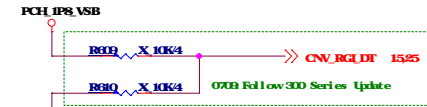
Internal Pull-down is disabled after RSMST# de-assert.

XIAL FREQUENCY SELECTION



This Signal has a Weak Internal Pull-down.
An External Pull-up is Required On this Strap Since 38.4 MHz XIAL is Not Supported On the PCH.
0 = 38.4 XIAL Frequency Selected (Default)
1 = 24MHz XIAL Frequency Selected

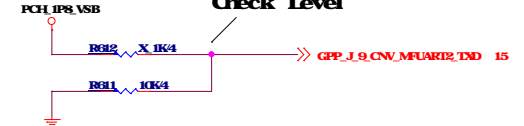
Midem Reference Clock Source Select



A Weak External Pull-up is Required
0 = Integrated CMA Enable
1 = Integrated CMA Disable

1.8V VCCSPH

need check level
Check Level



SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE
0 = VCCSPH IS CONNECTED TO 3.3V RAIL - DEFAULT
1 = VCCSPH IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD

Reserved



XIAL INPUT MODE
0 = XIAL INPUT IS SINGLE ENDED
1 = XIAL INPUT IS DIFFERENTIAL
PCH HAS INTERNAL 20K PD



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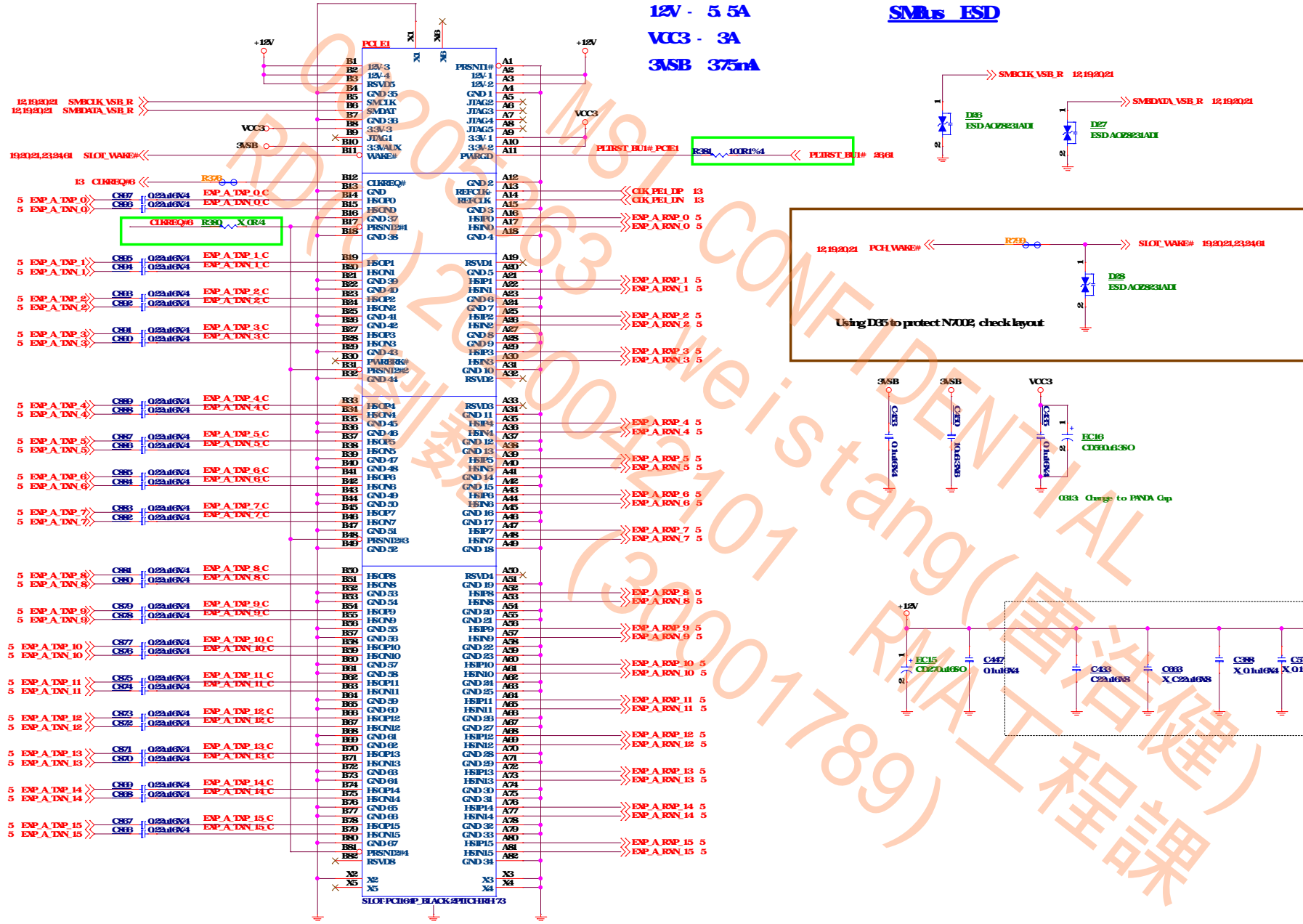
MS-7C79

Site Custom Document Description RCHStrap Rev 10/24/2010
Date: Monday, January 13, 2014 Sheet 88 of 90

PCI Express X16 Slot

12V - 5 5A
VCC3 - 3A
3VSB 375mA

SMBus ESD

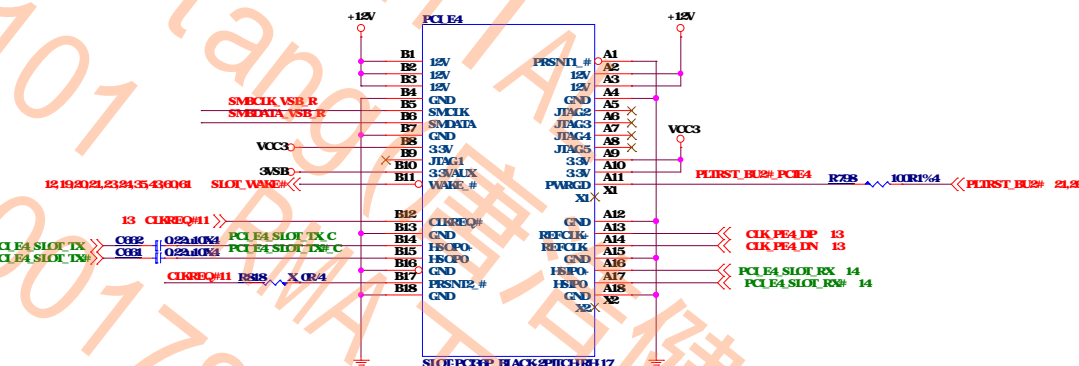
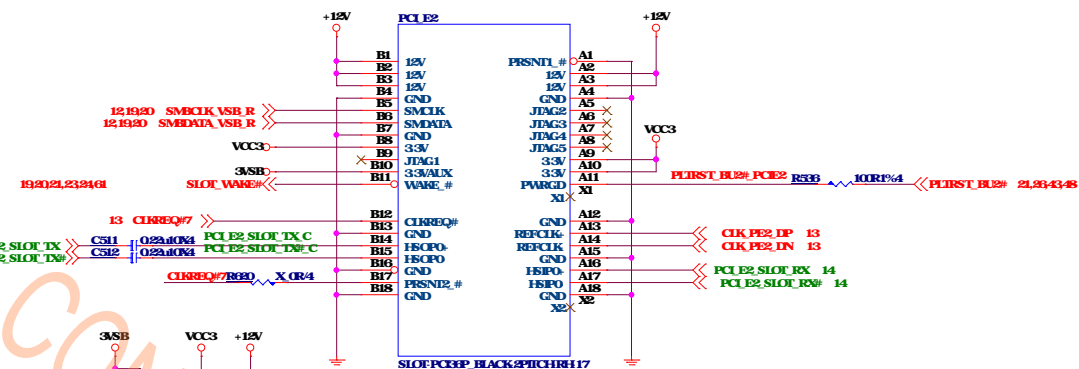


PCI/PCIE X1 Slot

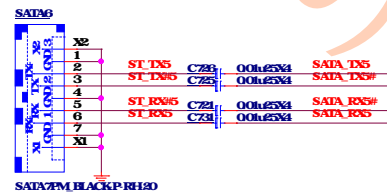
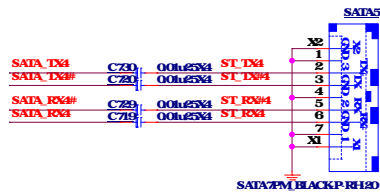
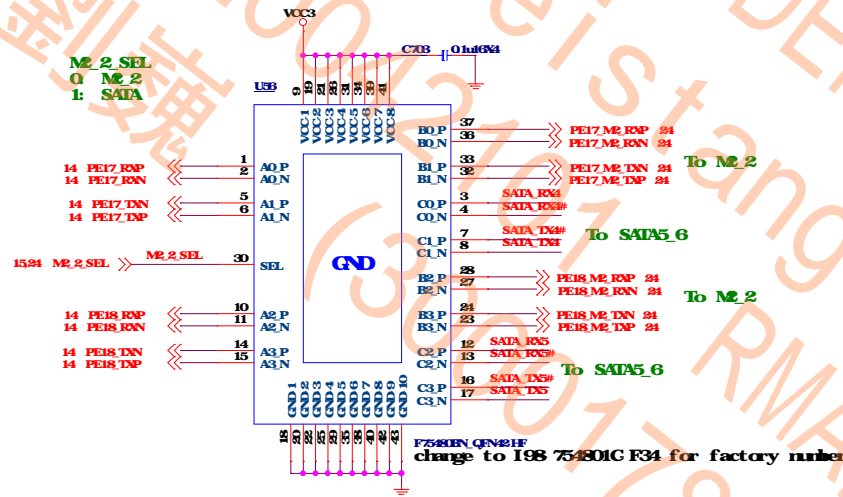
12V - 0.5A

VCC3 - 3A

3VSB - 375mA



SATA Connector

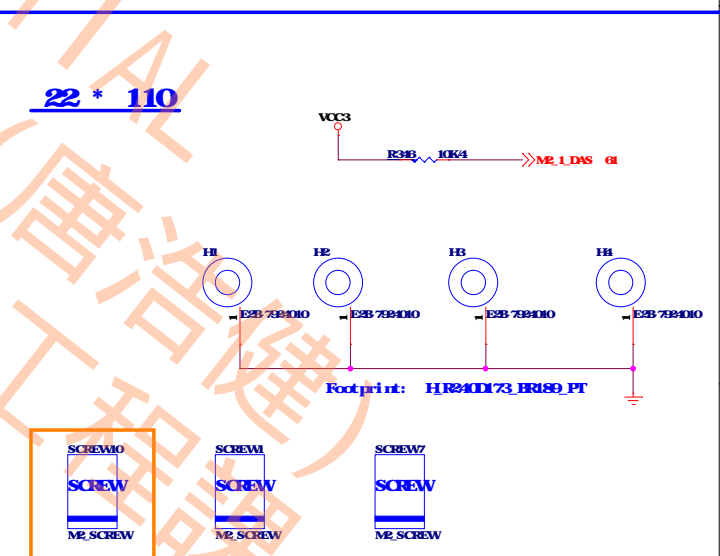
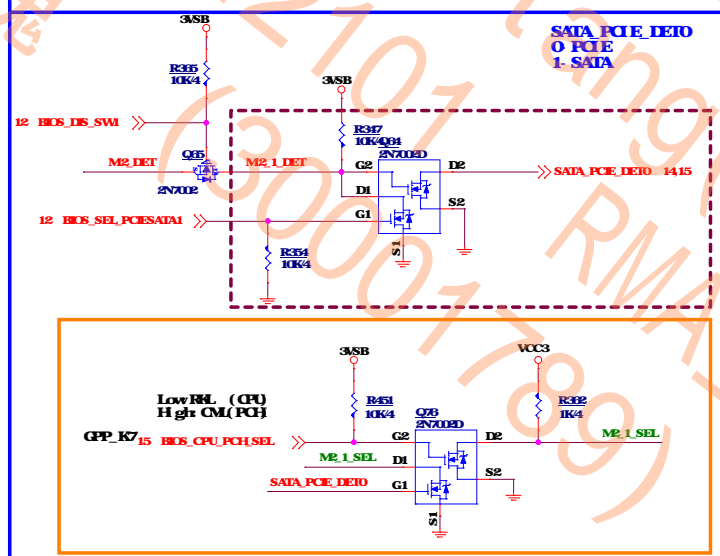
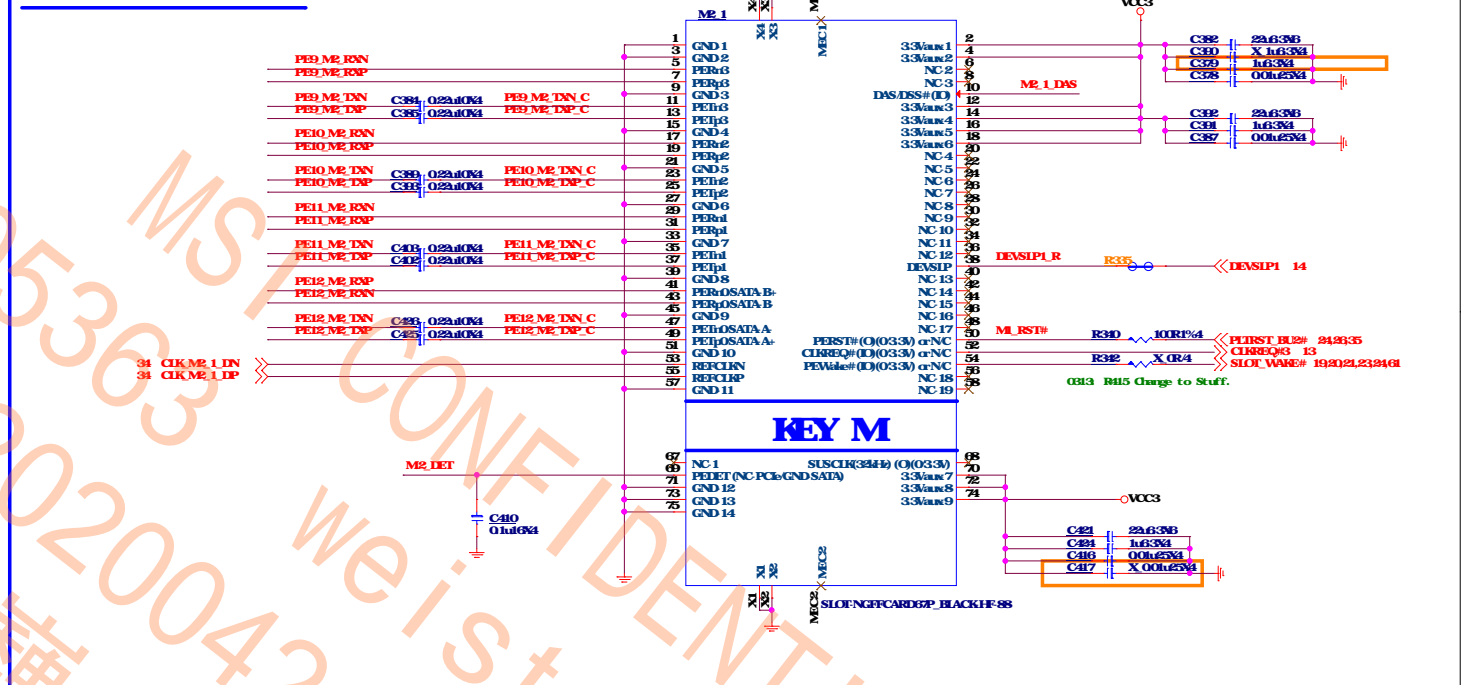
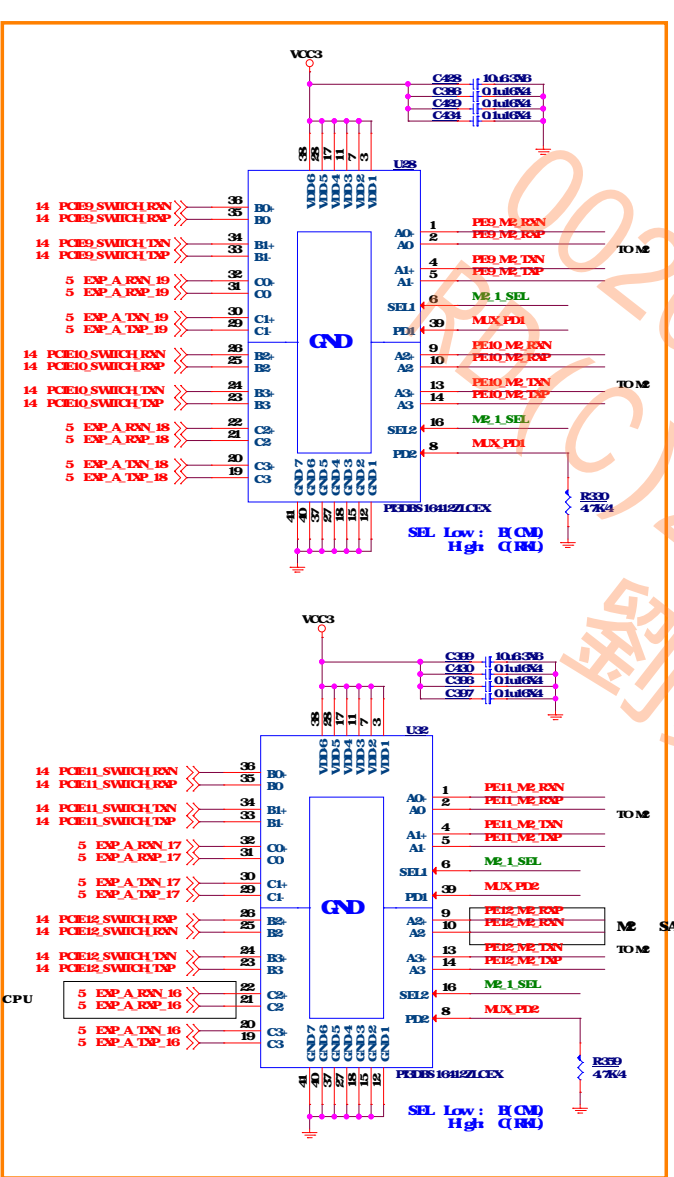


MICROSTAR INT'L CO., LTD

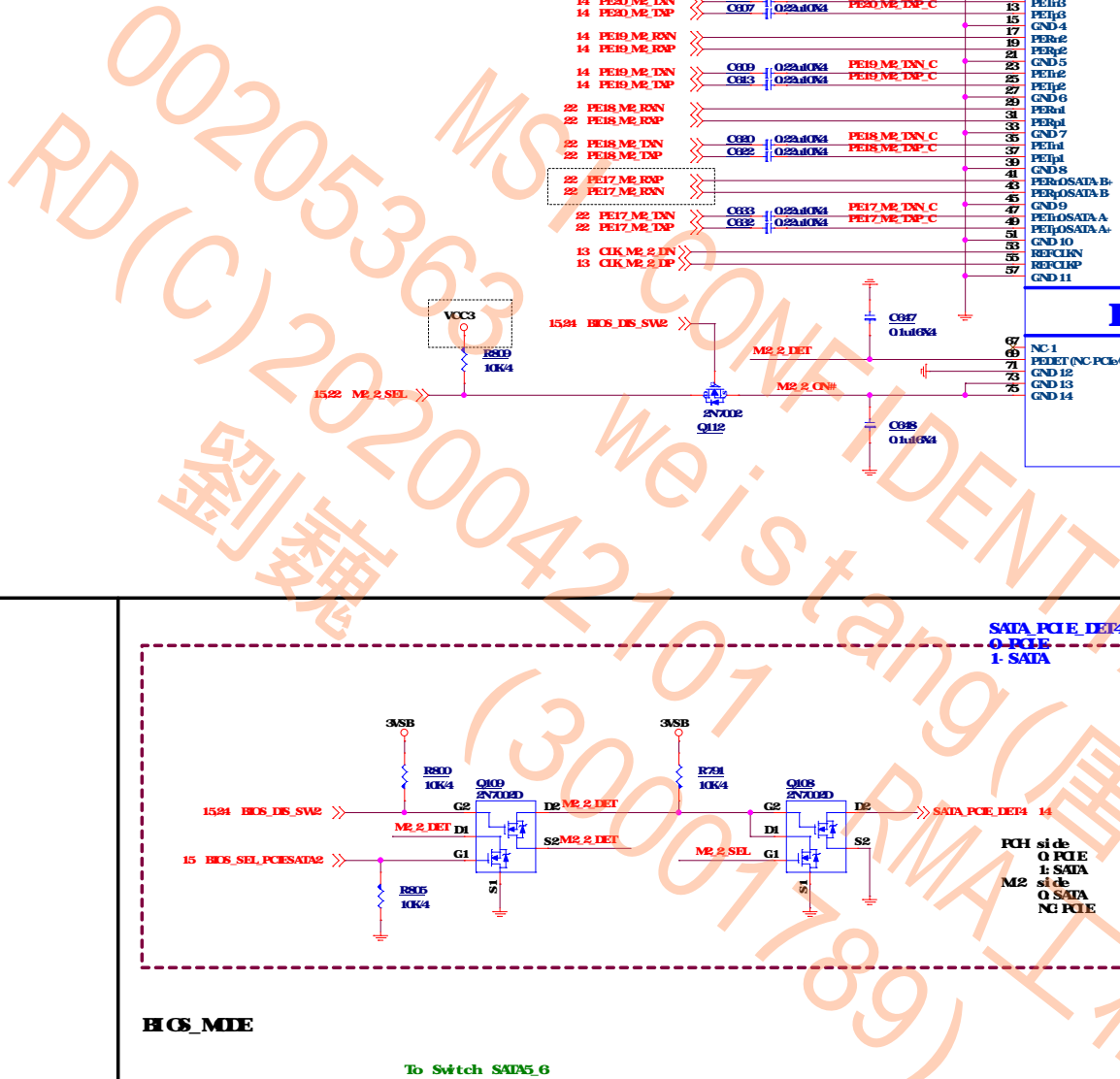
MS-7C70

Site	Document	Revision
Custom	SATA Connector	10
Date: Monday, January 13, 2020	Sheet 22 of 70	

M2 Connector



BIOS_DIS_SWI	BIOS_SEL_PCIE_SATAI	Mode
0	1	M2 SATA
0	0	M2 PCIe
GP1	GP1	AUTO

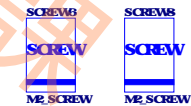
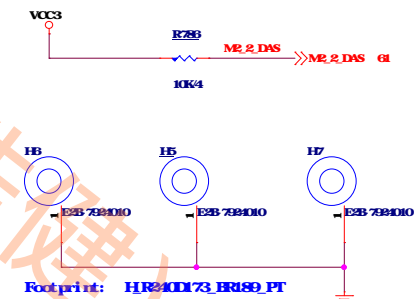



HCS_MDE

To Switch SATA5_6

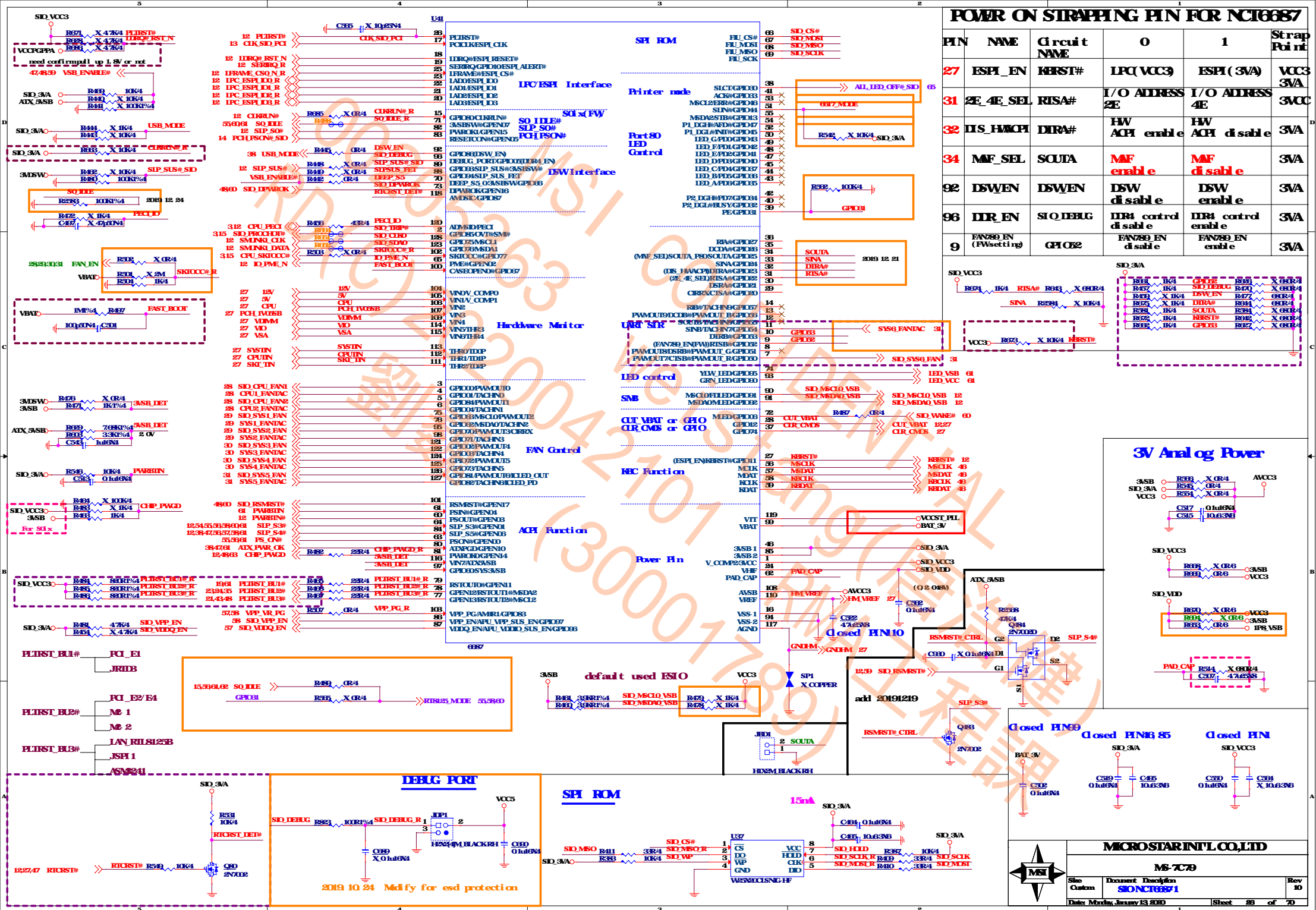
GP_G7	GP_G6	GP_G5		
HCS_DIS_SW2	M2_2_SEL	HCS_SEL_PCIE SATA2	Mode	SATA_PCIE_DET4
GPI (1)	GPI (1)	GPI (0)	AUTO	1
0	1	0	SATA5_6	1
0	0	1	M2 SATA	1
0	0	0	M2 PCIe	0

22 * 80



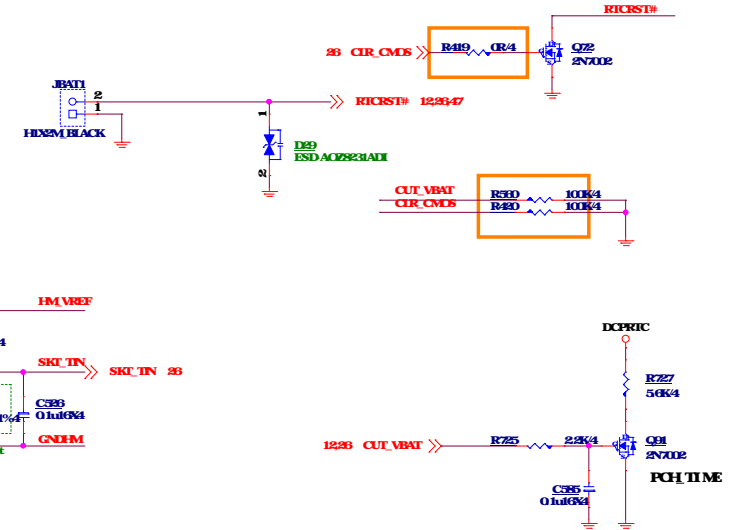
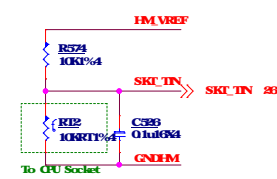
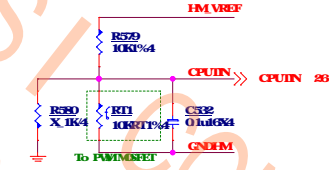
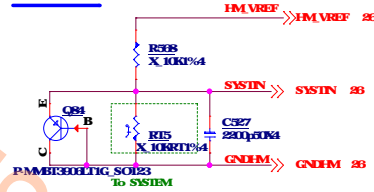


MICROSTAR INT'L CO., LTD			
MS-7C79			
Site	Document	Description	Rev
Custom	M8SL002		10
Date: March, January 23, 2020		Sheet 24 of 20	



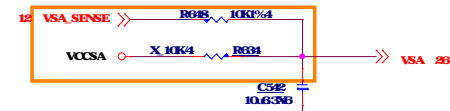
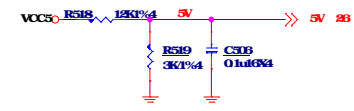
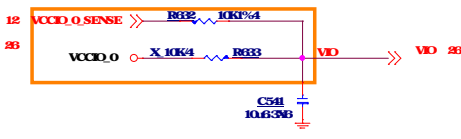
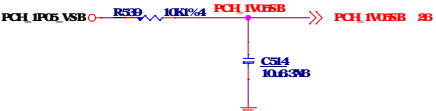
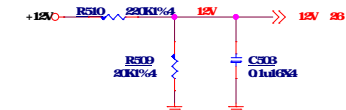
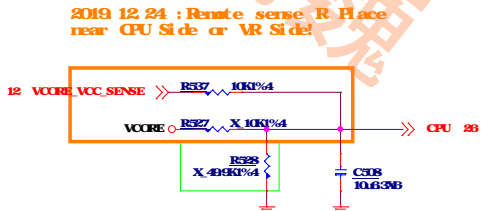
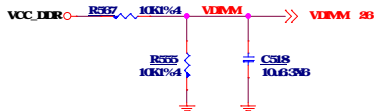
Serial Port 1

Thermal

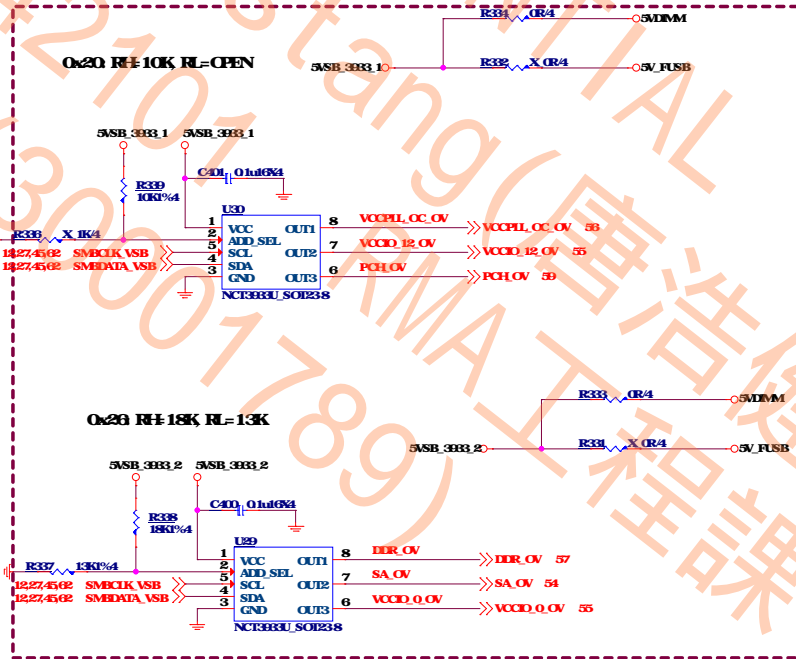


HWMonitor - Voltage

SIO HW Voltage Over 2V will Not Detect



VOLTAGE CONSOLE



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x2B	0x2C	0x2D	0x2E
RH(KOhm)	OPEN	39	3	22	13
RL(KOhm)	10	13	23	3	39
BUS_SEL	0%	25%	40%	60%	75%



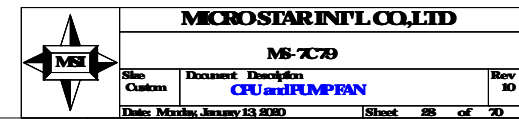
MICROSTAR INT'L CO., LTD

MS-7C79

Site	Document	Revision	Rev
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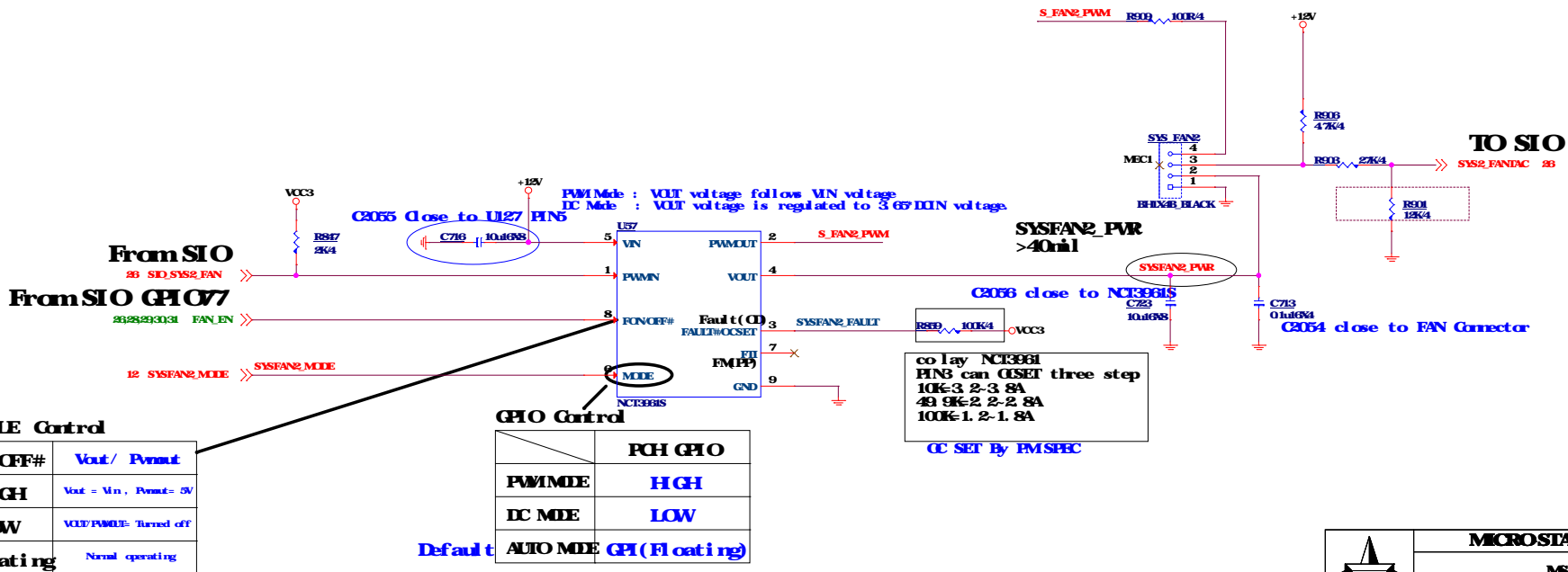
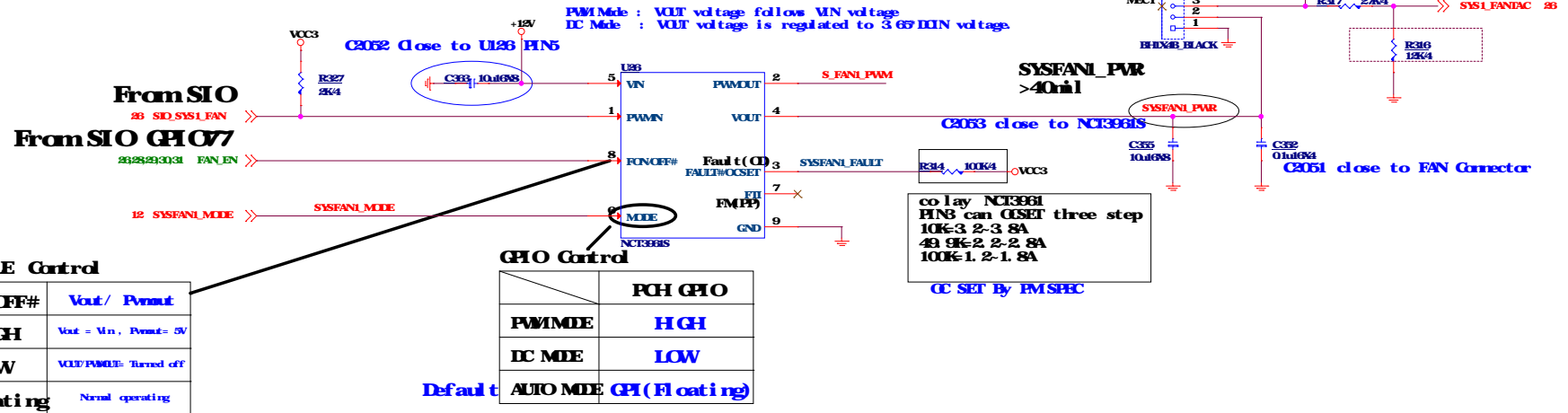
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2 FMBs can read FAN PWMDC MODE



TYPE M: 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO HIGH can switch PWM/DC Mode



1. Mode GPIO HCS can switch PWMDC MODE



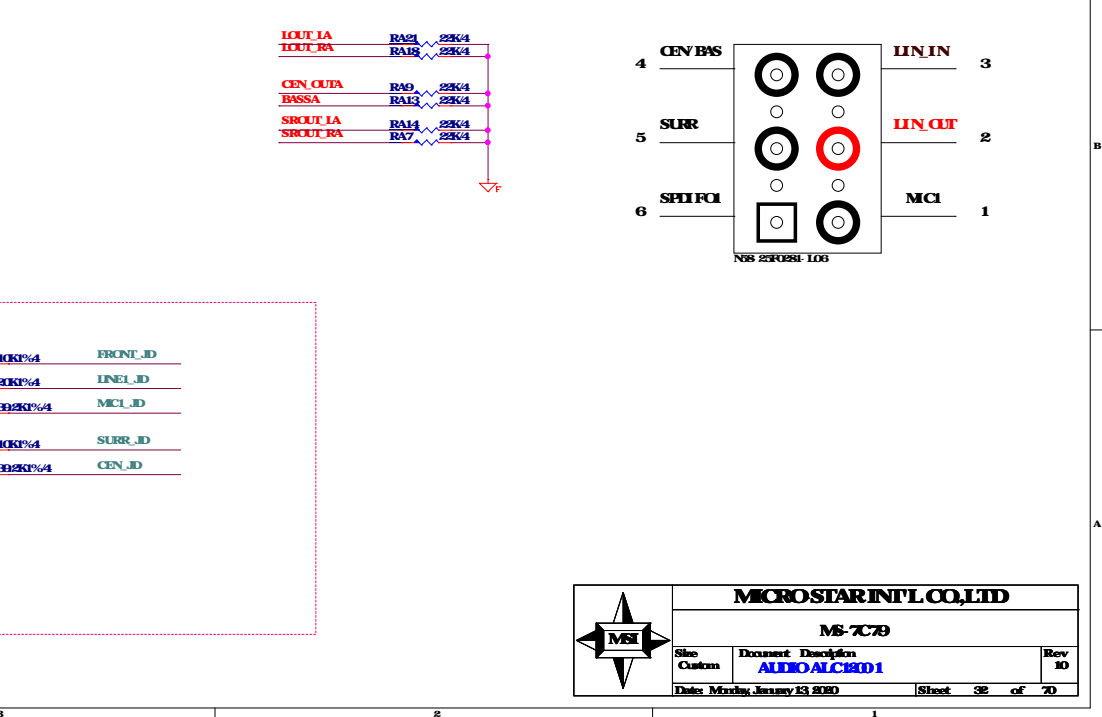
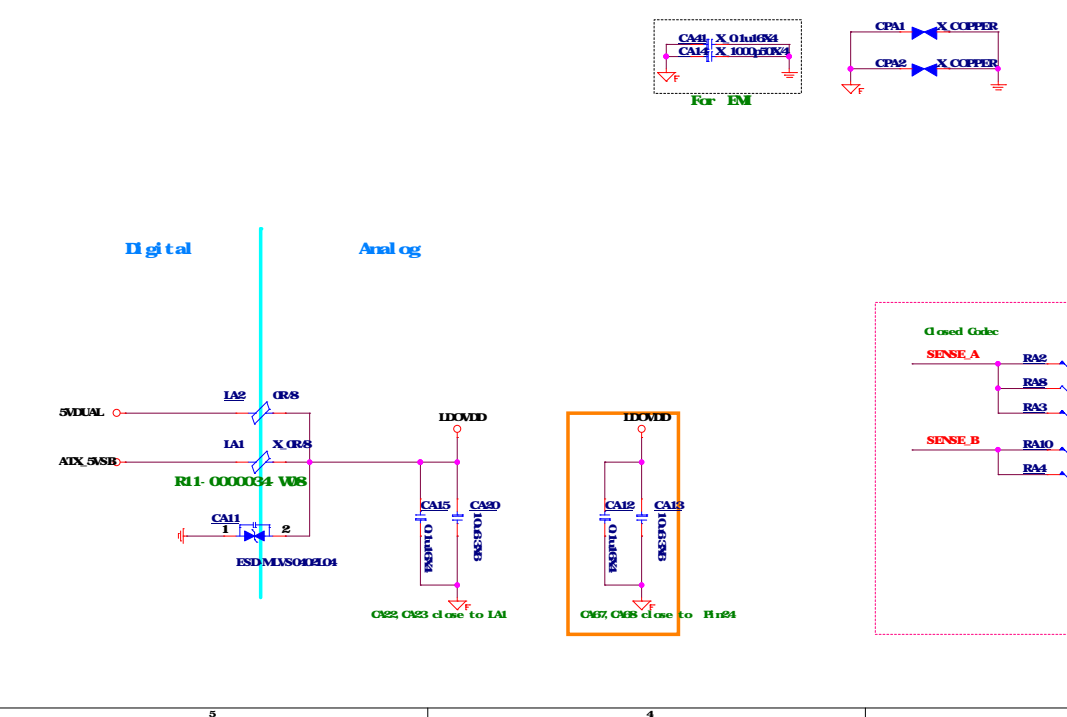
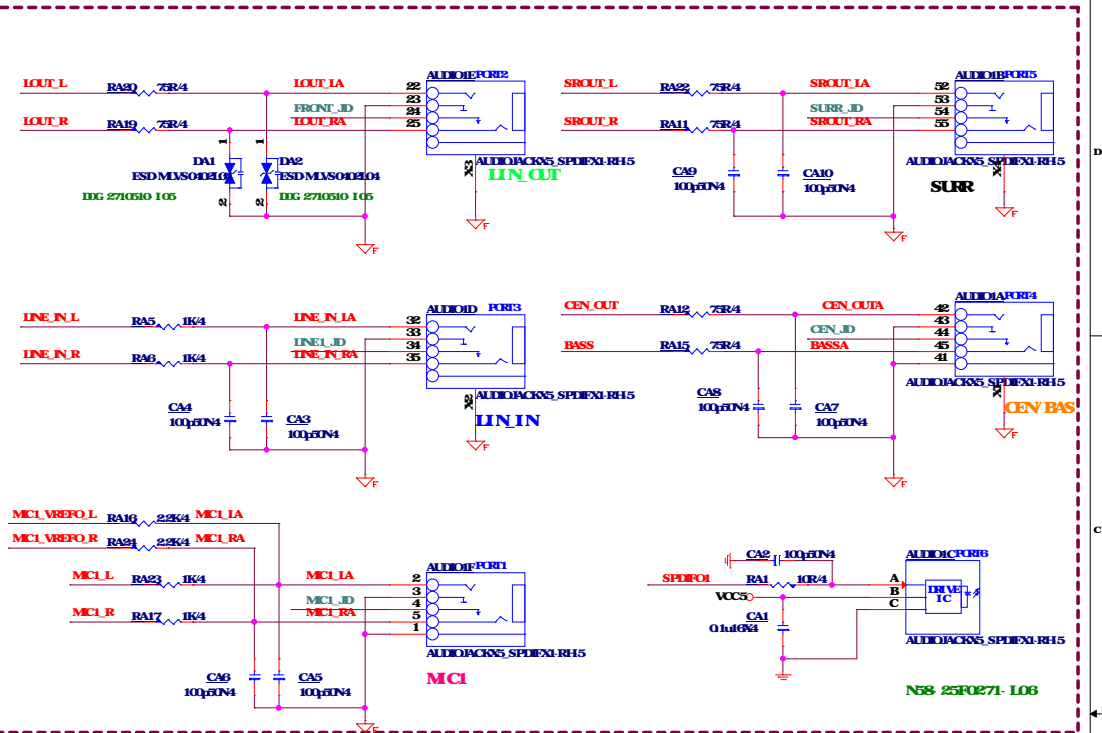
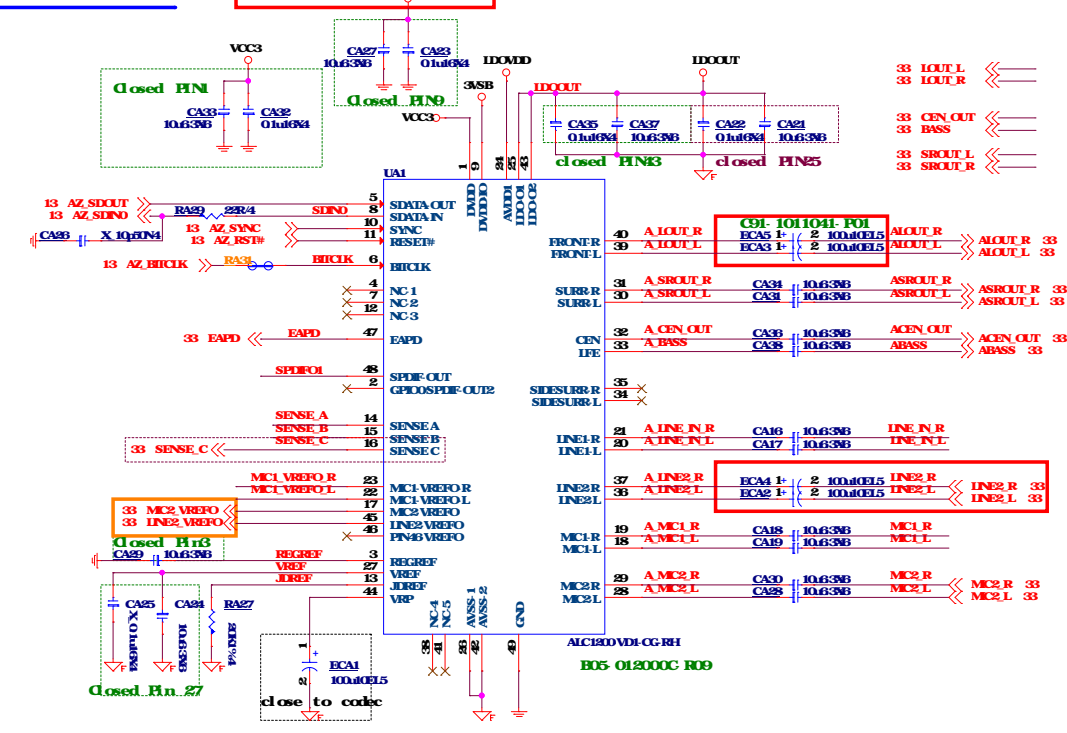
1. Mode GPIO HCS can switch PWMDC MODE

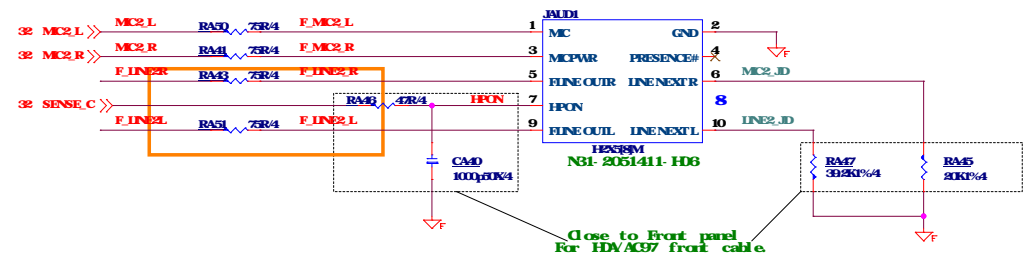
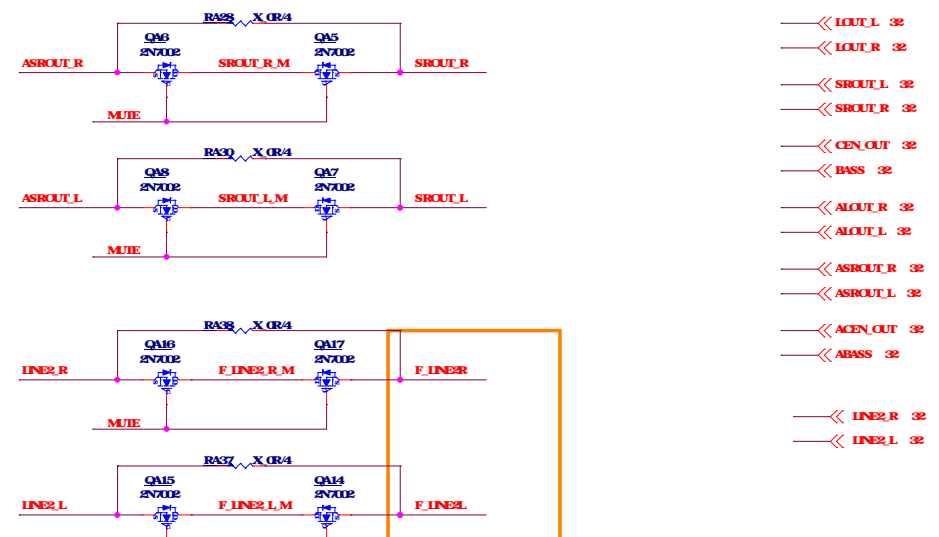
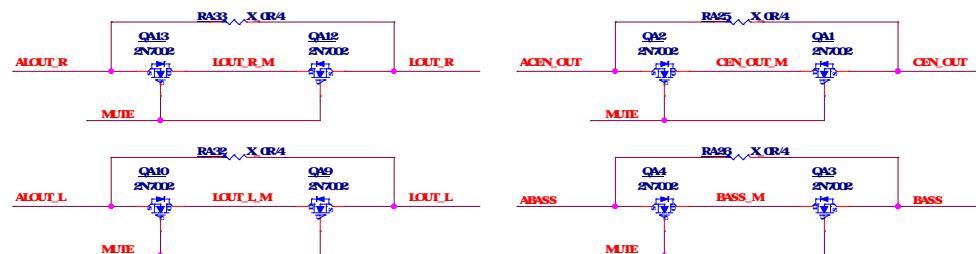


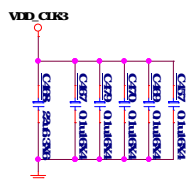
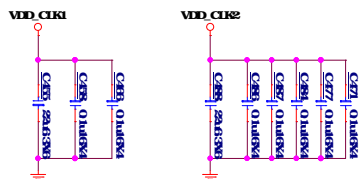
ALC1200

Follow RTH power well
need check

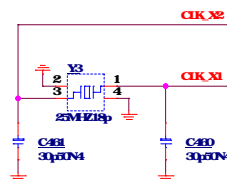
HN 1-12, 47-49 reference GND
others reference AGND



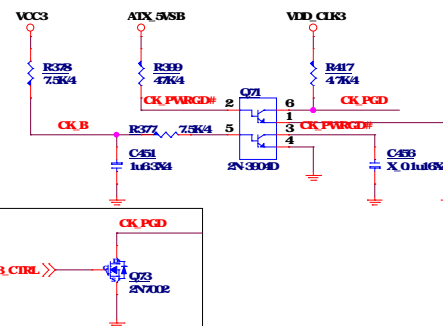
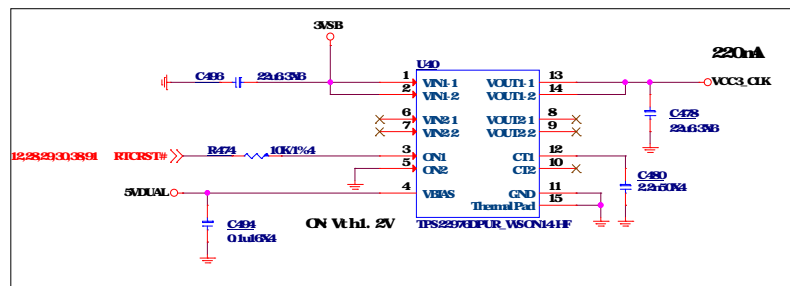
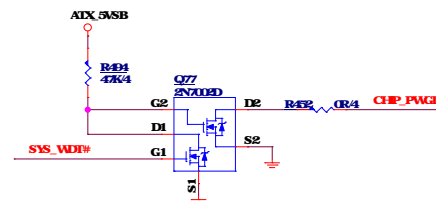
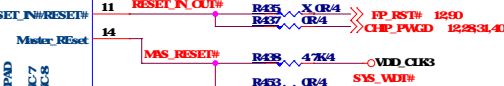
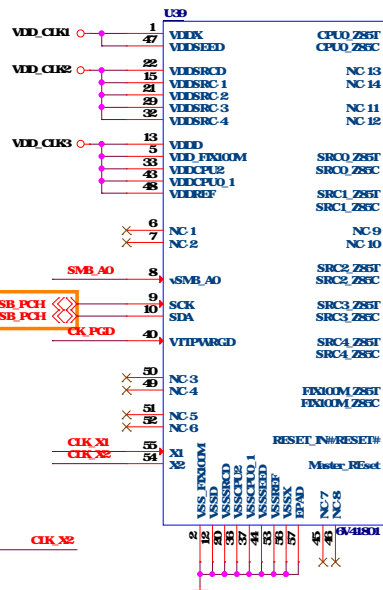
[illegible]



SMB_A0	ADDR
0	D2/D3
1	D8/D9



CPU_SEL	SRC_SEL	CPU(2 0)	SRC(5 0)	Notes
0	0	CPULL	CPULL	
0	1	CPULL	SRCPLL	Default
1	0	N/A	N/A	
1	1	SRCPLL	SRCPLL	

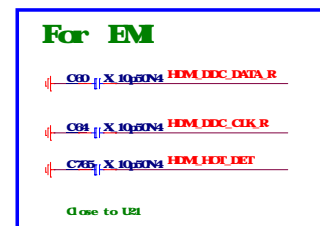
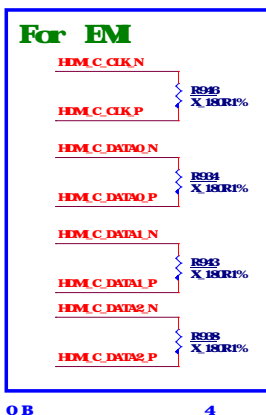
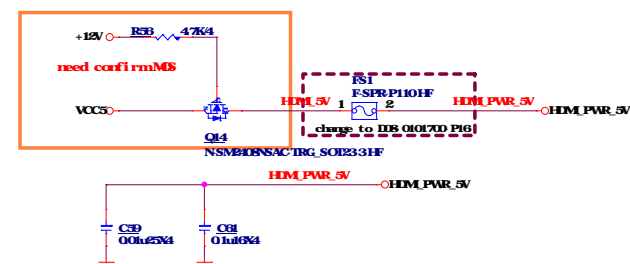
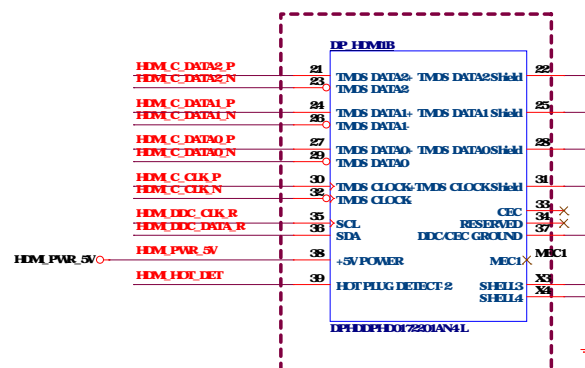
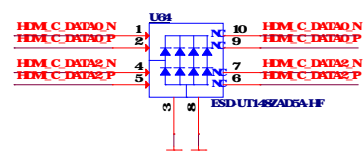
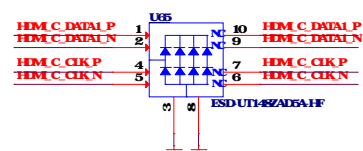
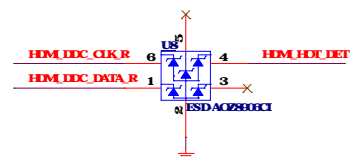


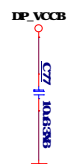
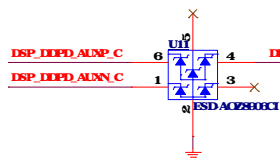
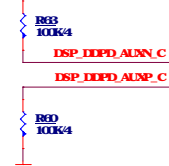
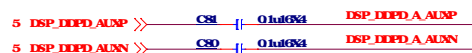
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Site Custom	Document Description 019 Clark Gen 6/4/8921	Rev M0
Date: Monday, January 13, 2020		Sheet 34 of 20

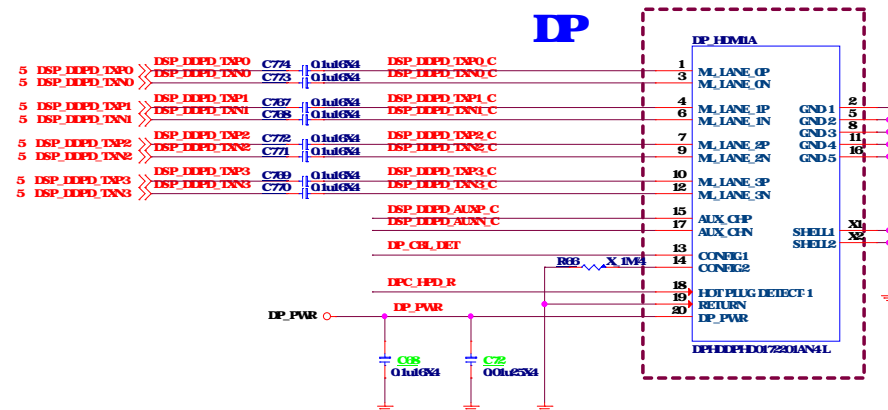
- Q 95V/ 1. 2A**







198 35320C N62

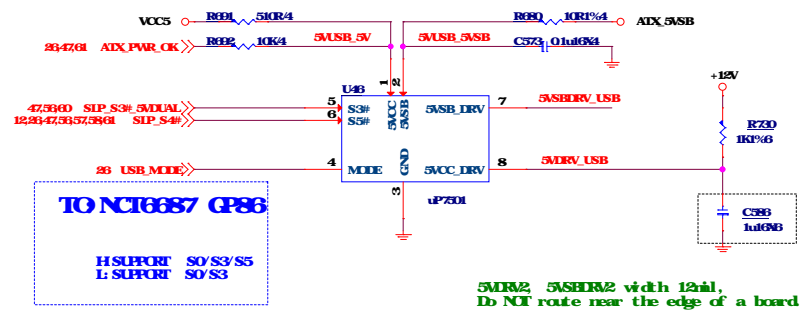


MS-7C79

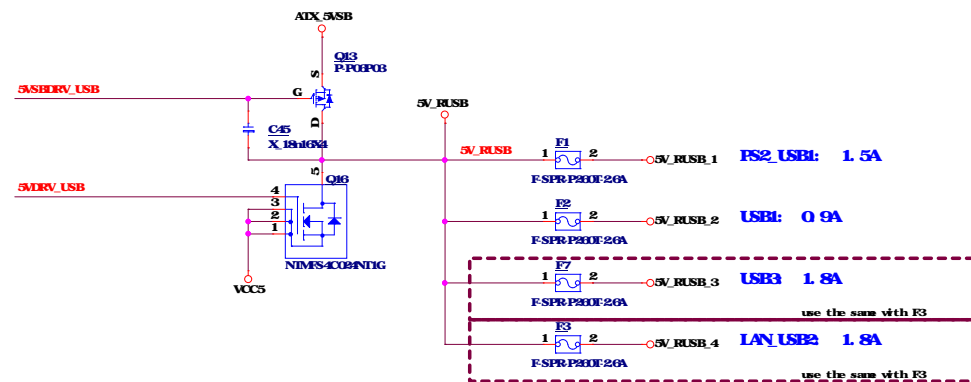
Rev
10

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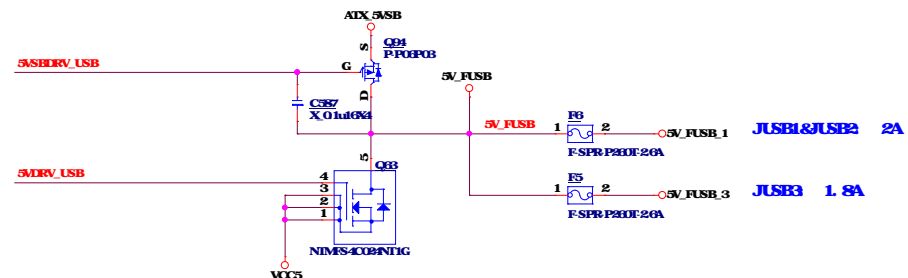
USB Power



Rear USB Port Power



Front USB Port Power

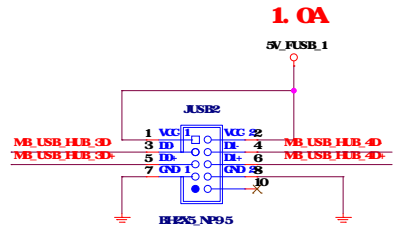
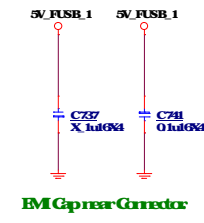
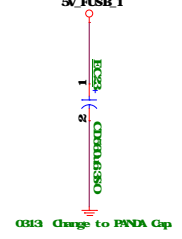
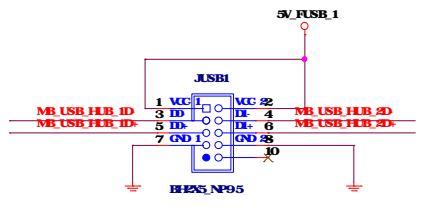
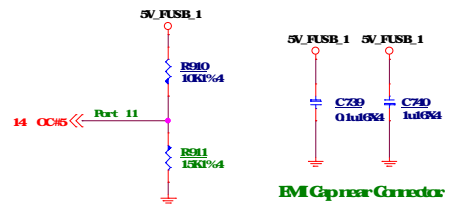
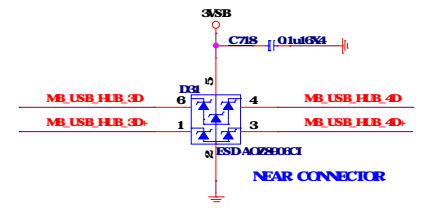
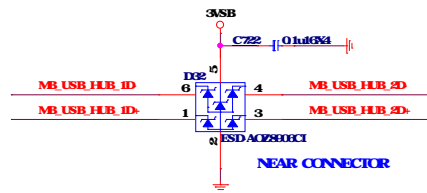


MICROSTAR INT'L CO., LTD

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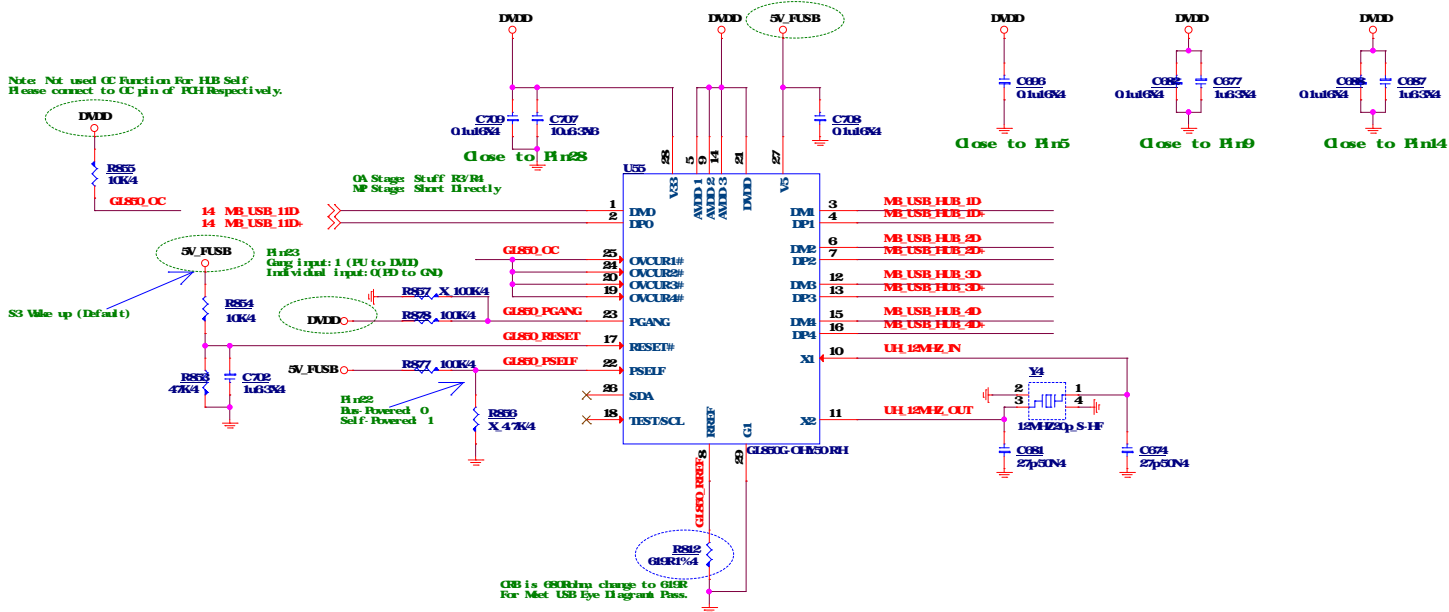
Site Custom	Document Description USB Power	Rev 10
Date: Monday, January 13, 2020		Sheet 36 of 70

Front USB2 0



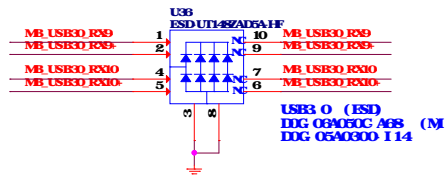
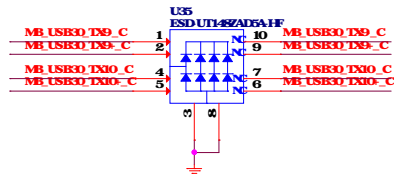
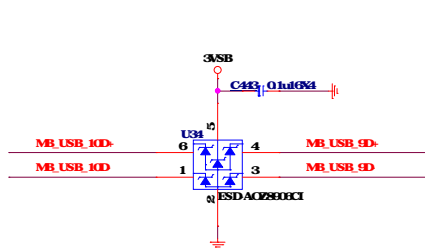
GL50G USB20HUB

Note: Please connect to USB Power Source.

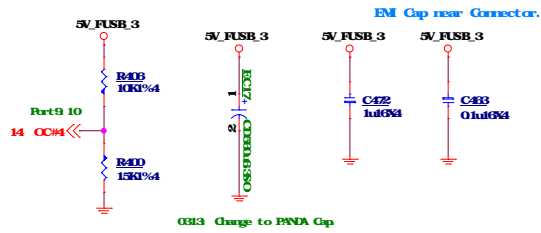


MICROSTAR INT'L CO., LTD			
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Site	Document	Revision	Rev
Custom	Front USB20		10
Date: Monday, January 13, 2003		Sheet	39 of 70

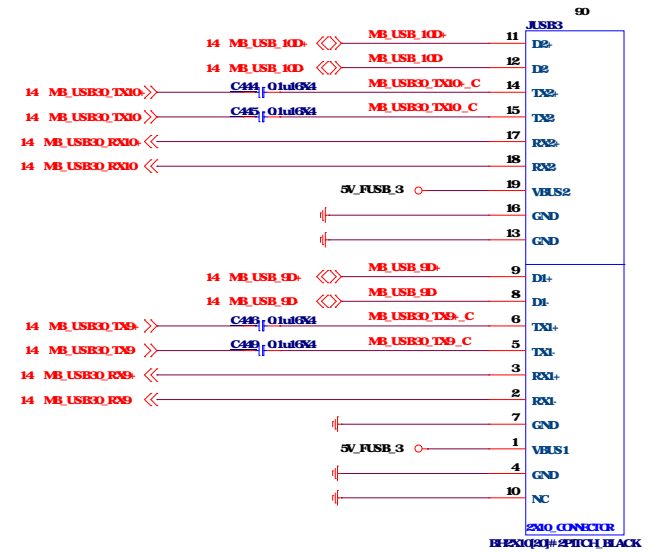
Front USB3 1 Gen1



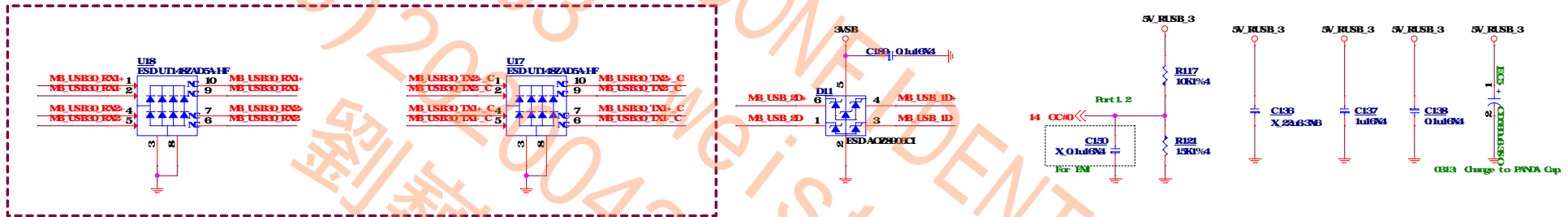
USB3 1 (ESD)
IDG 0890C03 A68 (M)
IDG 0540300 I 14



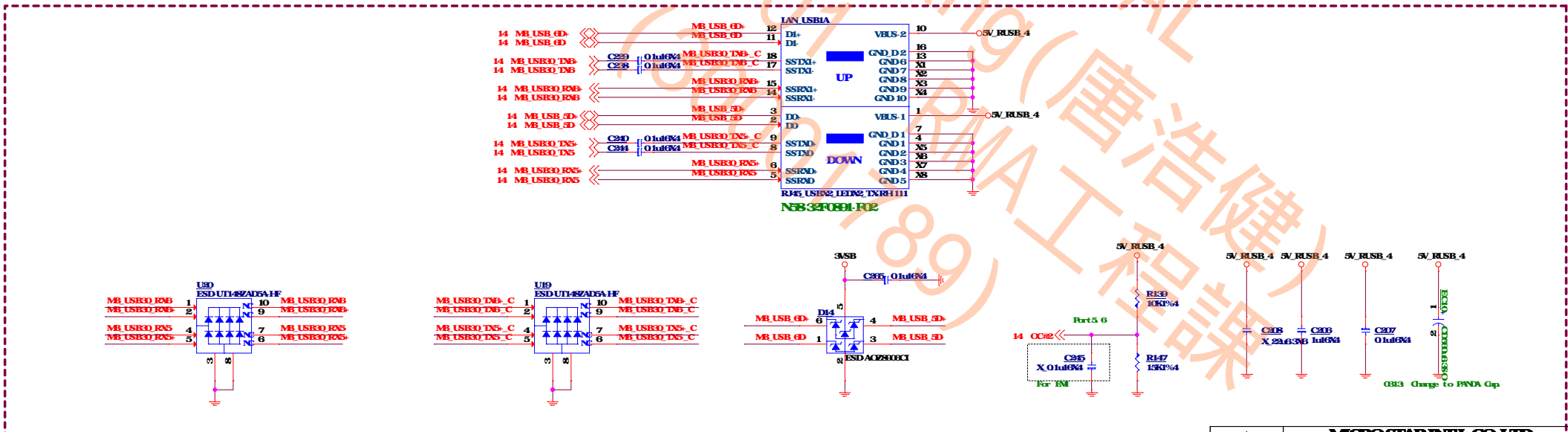
EM Cap near Connector.



Rear USB3 1 Gen1



Rear LAN USB3 1 Gen1



2019.12.18

14 MR_USB30_TX3
14 MR_USB30_TX3
14 MR_USB30_RX3
14 MR_USB30_RX3

C125 022a0K4 MR_USB30_TX3_C-2
C190 022a0K4 MR_USB30_TX3_C-3
C113 022a0K4 MR_USB30_RX3_C-9
C117 022a0K4 MR_USB30_RX3_C-8

TX1_EN 30
TX1_RXEN 11
TX2_EN 29
TX2_SWB 12
TX3_EN 27
TX3_SWB 18
TX4_EN 35
TX4_SWB 22
TX5_EN 39
TX5_SWB 26
TX6_EN 40
TX6_SWB 31

Internal 30K Pull-up
Internal 100K Pull-up and 20K Pull-down

U4
VDD1
VDD2
VDD3
VDD4

24 USB30_TXDP_C C112 022a0K4 USB30_TXDP
23 USB30_TXDN_C C116 022a0K4 USB30_TXDN
17 USB30_RXDP_C C123 033a0K4 USB30_RXDP
18 USB30_RXDN_C C119 033a0K4 USB30_RXDN

BQA
EQB
FQA
FGB

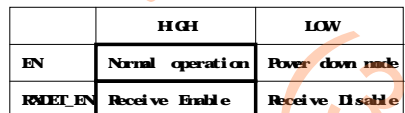
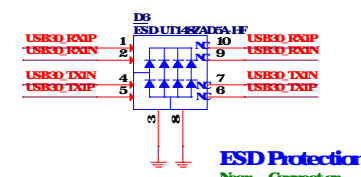
26 TX1_EQA
15 TX1_EQB
27 TX1_FQA
14 TX1_FGB

Internal 100K Pull-up and 20K Pull-down

USB30_RXDP 19B 200K%4
USB30_RXDN 19B 200K%4

NEP5Q100M17AG

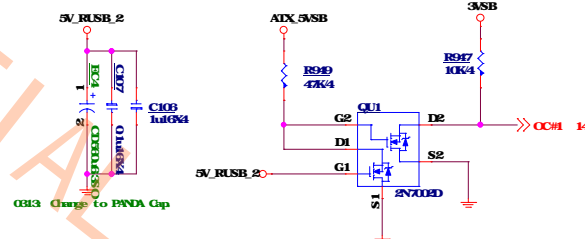
19B 110Z0C 005



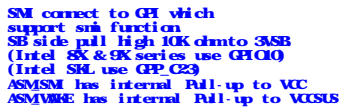
```

UN_EQA setting Floating , RI15 NC
UN_EQB setting 68K ohm to GND , RI17 68K ohm
UN_FGA setting 0 ohm to GND RI11 NC, RI12 0 ohm
UN_FGB setting Floating , RI14 NC
UN_SVA and UN_SVB setting Floating RI19 RI21 NC

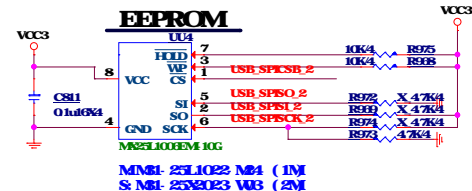
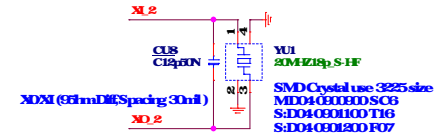
```



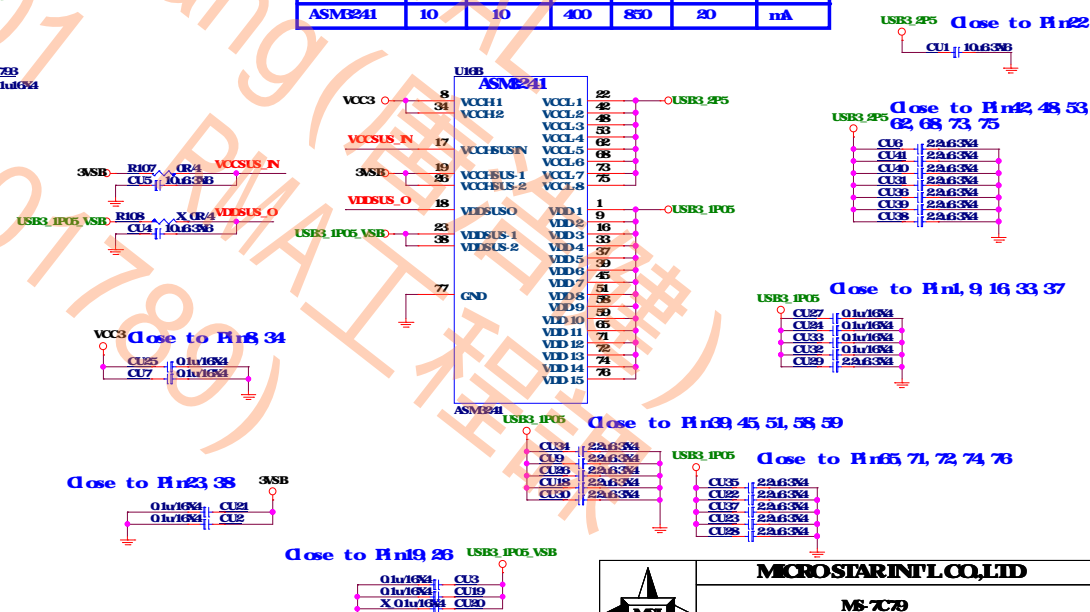
Symbols	Parameter	Min	Typ	Max	Unit	Remark
V _{TH_POR}	Threshold voltage for PORST pins	1.38	1.6	1.8	V	Use Q 22a Gr2 use
t _{OCI}	OCI* ready after Suspend/ Power Ready			12	ms	
t _{WR}	Write time for Suspend and normal Power Ready			10	ms	
t _{POWER}	Timing for all normal power Ready	50			ms	Note 1
t _{PORST1}	Timing for all normal Power Ready to Power On Reset (when suspend power domains are existed)	10		80	ms	
	Timing for all normal Power Ready to Power On Reset (when suspen powers connect to normal power directly)	60		80	ms	



1) USB3.1 to Connector Total Length < 1.5'

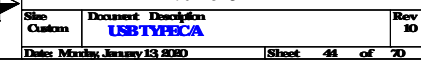


	3.3V	3.3VSUS	2.5V	1.05V	1.05VSUS	Unit
ASMB241	10	10	400	850	20	mA

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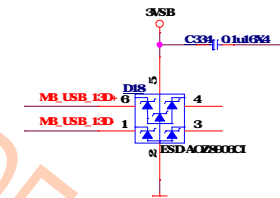
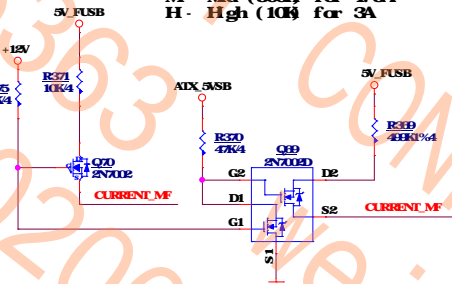
1.5A under S3 node
3A under S0 node



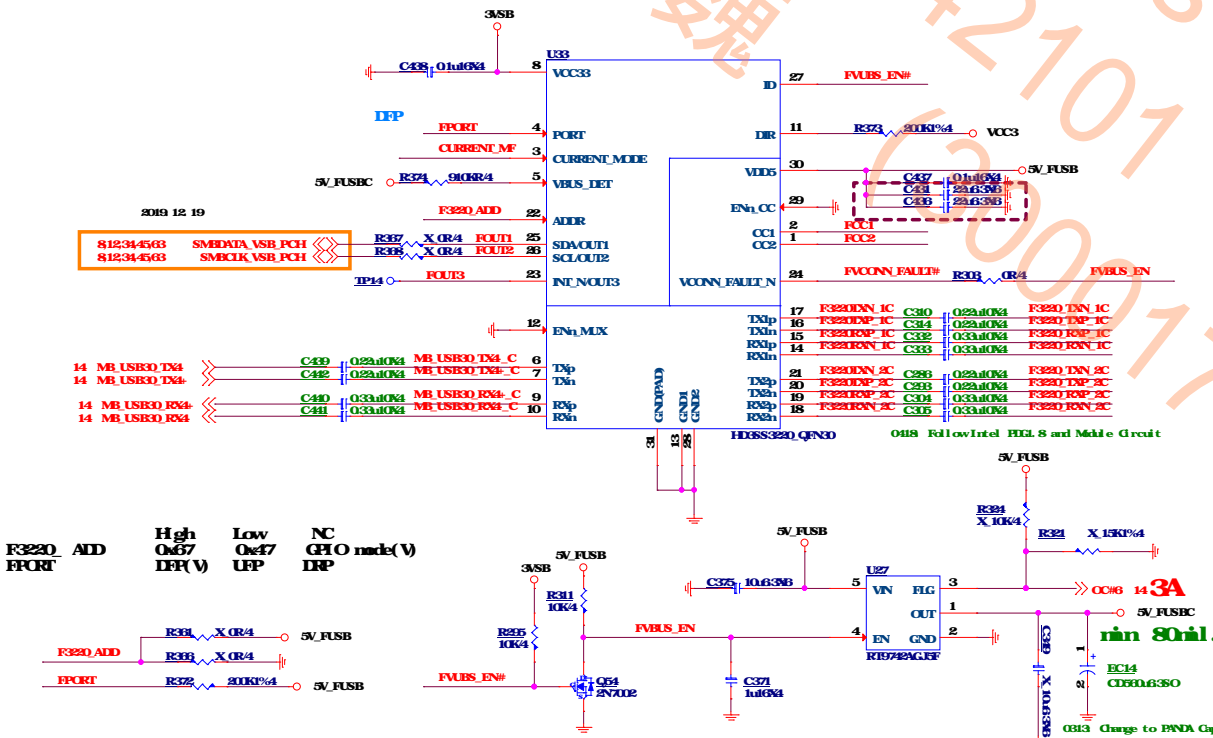
Current Mode

3A under S0 mode
1.5A under S3 mode

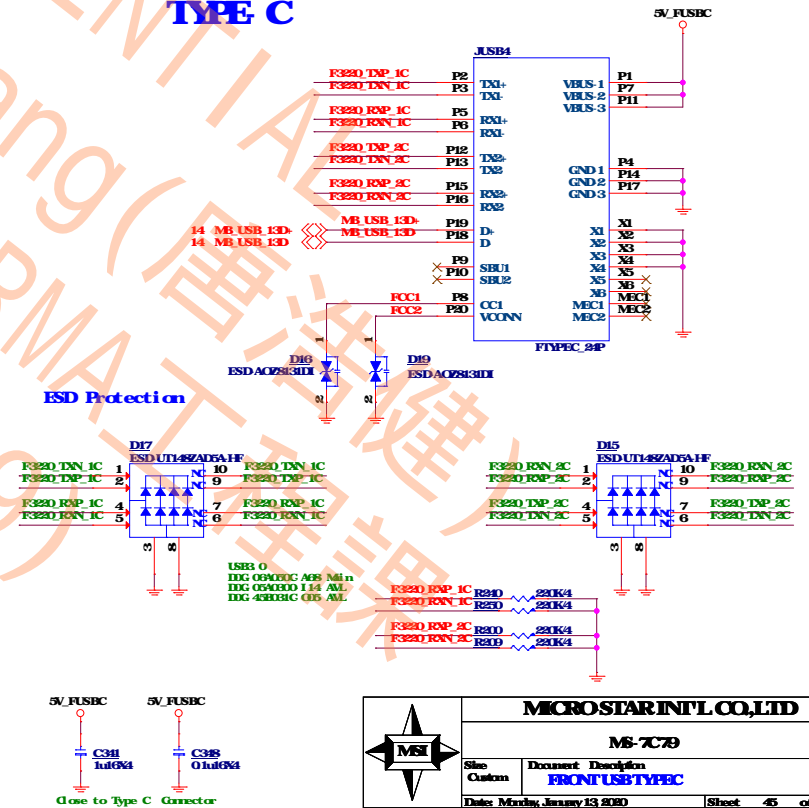
L- Default for 900mA
M- Mid (500K) for 1.5A
H- High (10K) for 3A



USB Type C MIX with Configuration Channel (CC)

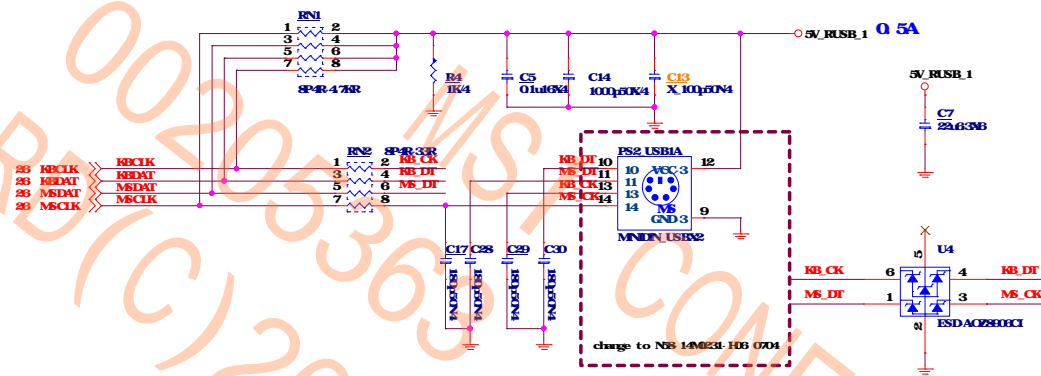


TYPE C

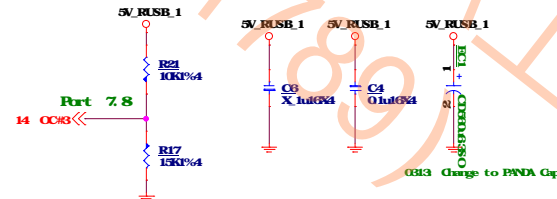
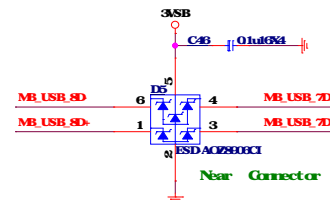
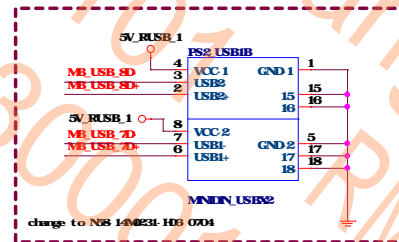
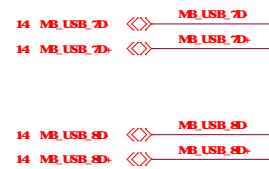


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Custom	FRONT USB TYPE C	B0	
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PS2 Keyboard & Mouse Connector



PS2 USB2 0

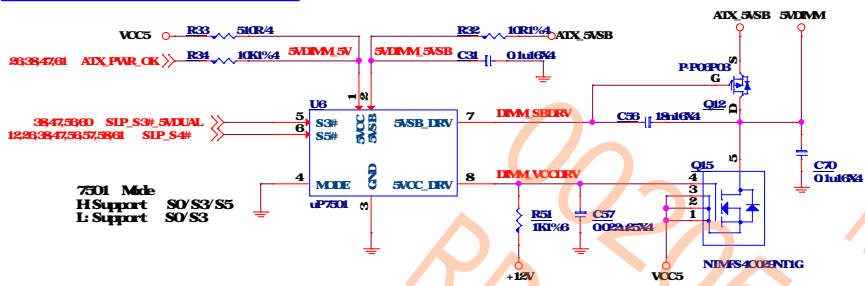


MICROSTAR INT'L CO., LTD

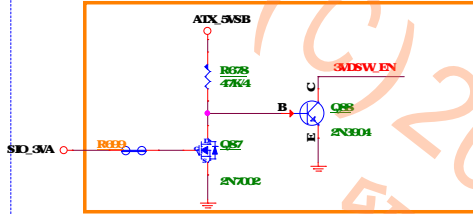
MS-7C79

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Custom	PS2 USB1	10
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5VIMMFOR DDR

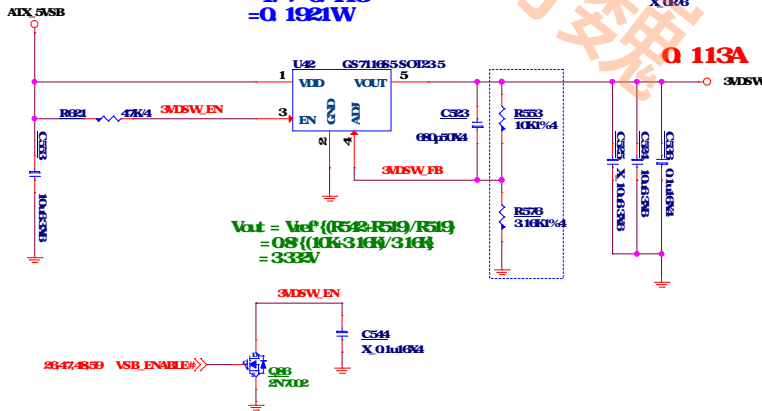


For S5 -> G3 3VSWEN Bounce issue



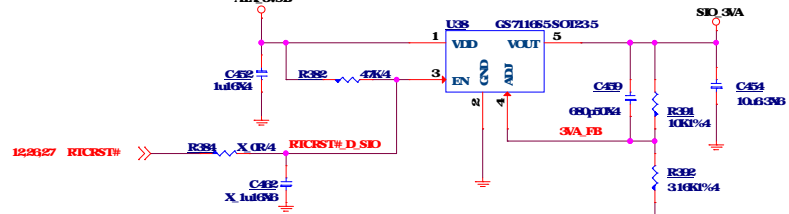
$$\text{Power Loss} = (V_{in} - V_{out}) \cdot I_{out} \\ = (5.3 - 3) \cdot 0.113 \\ = 1.7 \cdot 0.113 \\ = 0.1921W$$

Resverd
0.113A

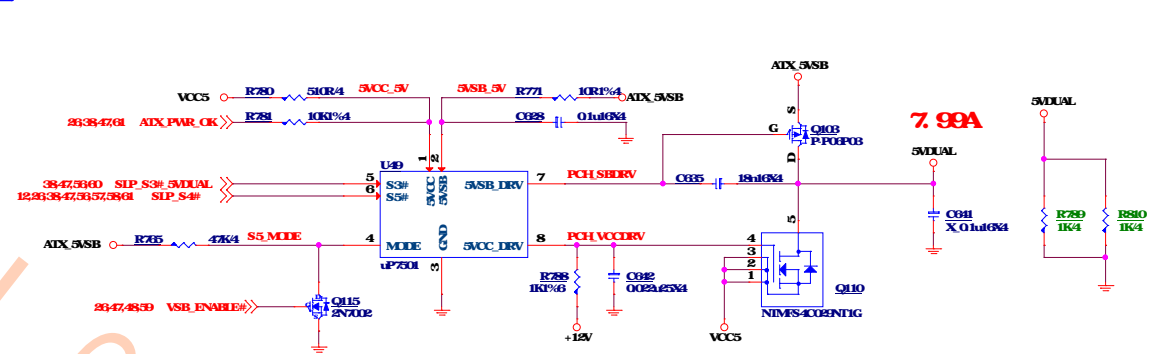


$$V_{out} = V_{in} \cdot \left(\frac{R_{57} + R_{58}}{R_{57}} \right) \\ = 0.8 \cdot \left(\frac{10K + 31K}{31K} \right) \\ = 3.33V$$

$$\text{Power Loss} = (V_{in} - V_{out}) \cdot I_{out} \\ = (5.3 - 3) \cdot 0.04 \\ = 1.7 \cdot 0.04 \\ = 0.068W$$

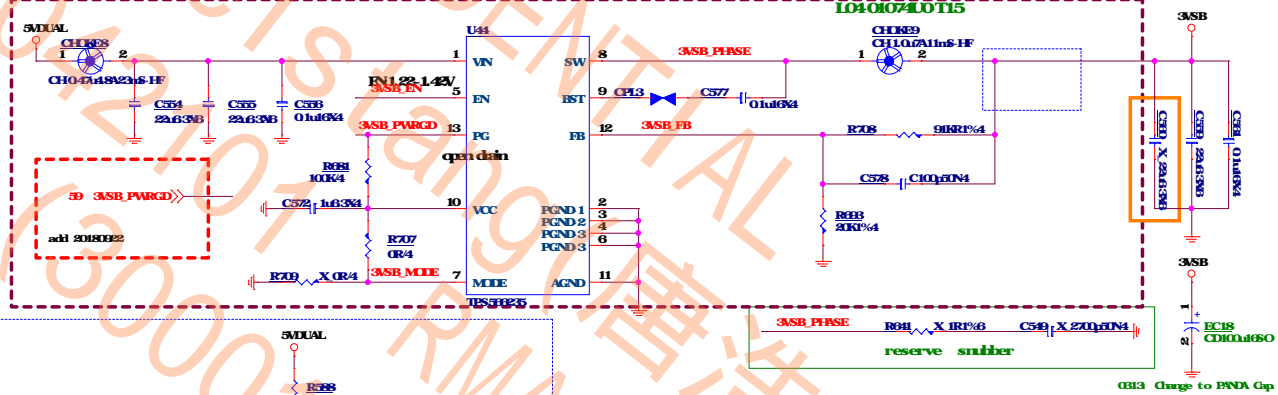


5VDUAL



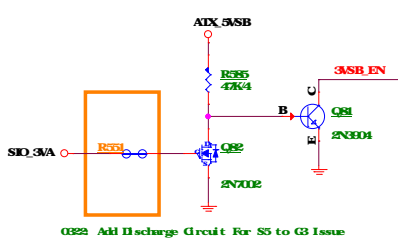
3VSB

$$I_{rrms} = I_{out} \cdot \sqrt{f \cdot (V_{out}/V_{in}) \cdot (1 - (V_{out}/V_{in}))} \\ = 4.98 \cdot \sqrt{0.474} \\ = 2.35A$$



$$V_{out} = V_{in} \cdot \left(\frac{R_{57} + R_{58}}{R_{57}} \right) \\ = 0.8 \cdot \left(\frac{10K + 31K}{31K} \right) \\ = 3.33V$$

For S5 -> G3 3VSB EN ISSUE

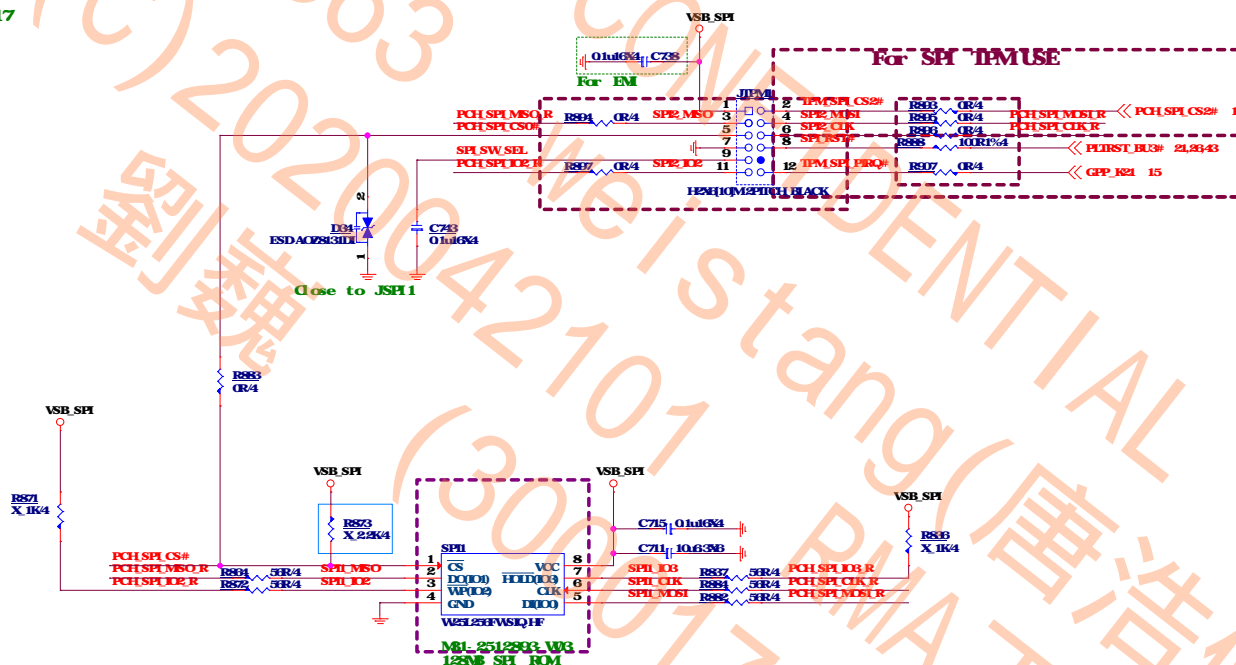
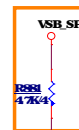


Vmode(VP25 MODE)	0-0.3V	0.3-1.2V	>1.2V
Rmode	OR	100K-150K	To VCC(recommend) or R-400K
Operating Mode	Eco Mode	Out-CF-Audio	FCOM



MICROSTAR INT'L CO., LTD			
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Custom	ACH		10
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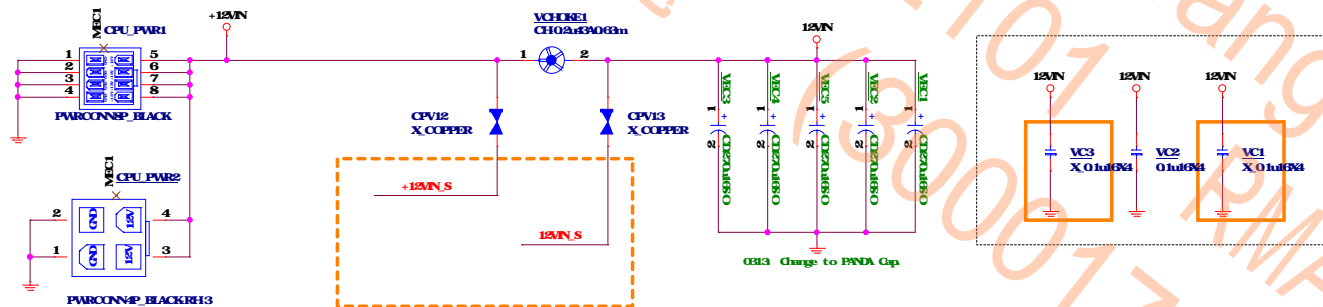
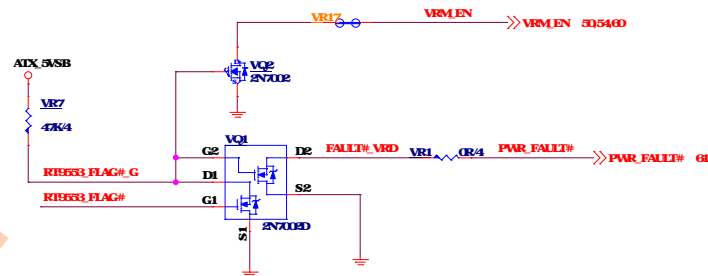
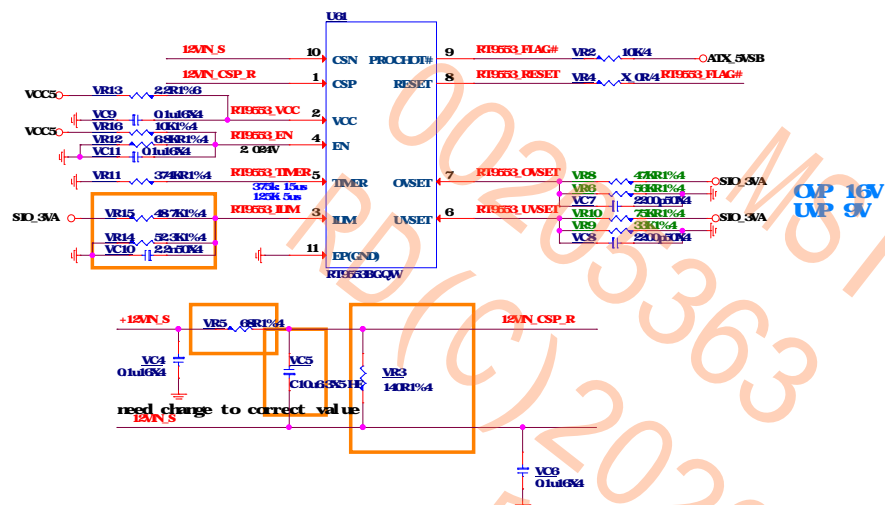
For TL624 1.
DEEP Mode : Stuff D18/R2517
DSWMode : Stuff D18/D19/R2517



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Site Custom	Document Description BIOS ROM	Rev M
Date: Monday, January 13, 2020		Sheet 48 of 70

CCP 45A
VILIM1. 711V



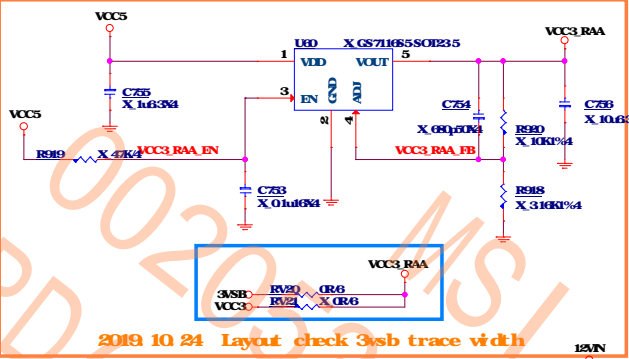
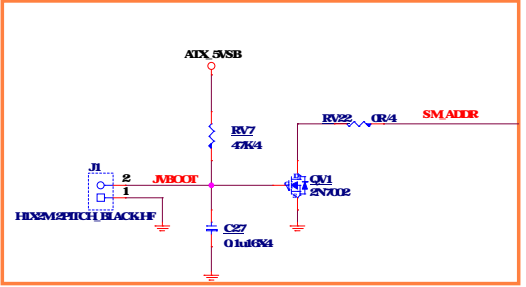
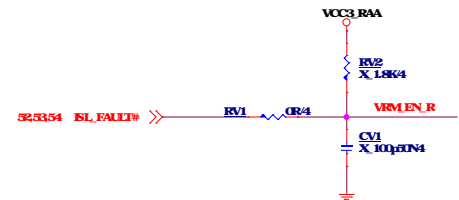
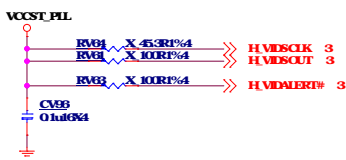
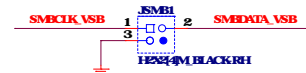
MICROSTAR INT'L CO., LTD

MS-7C79

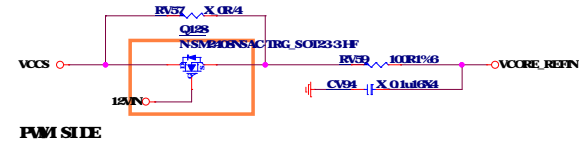
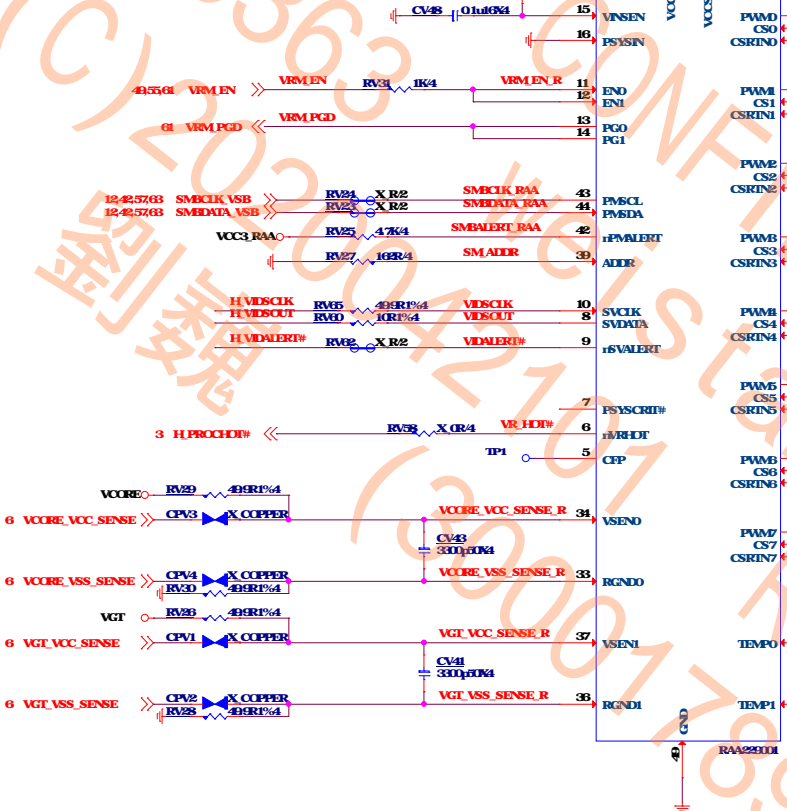
Site	Document Description	Rev
Custom	12VIN Current Detect	10
Date: Monday, January 13, 2020	Sheet 49 of 70	

VCORE ICC Max 245A
IL: 1.1 nA
VGT ICC Max 35A
IL: 4 nA

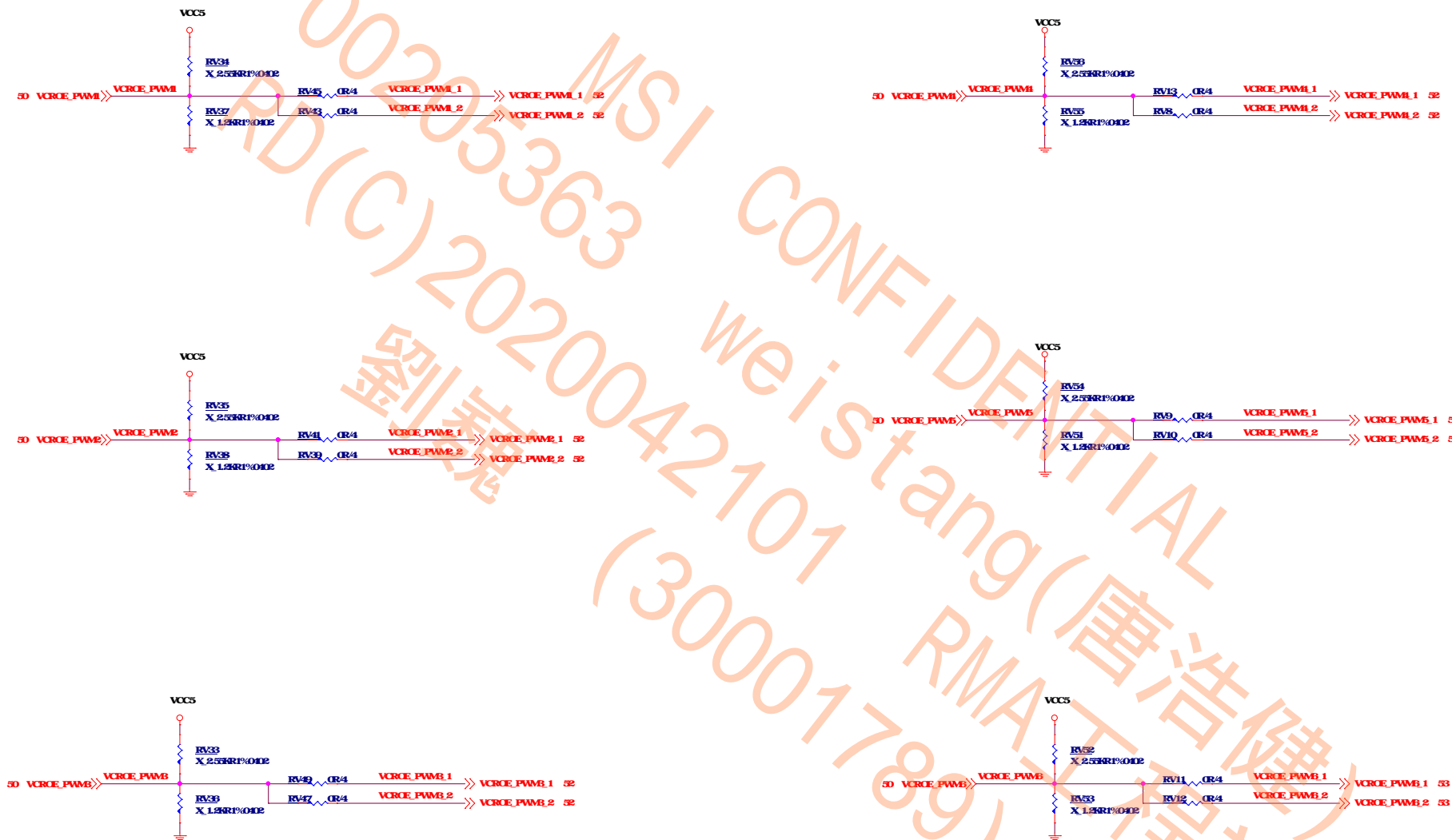
SMB Address: 080



2019 10 24 Layout check 3v3b trace width



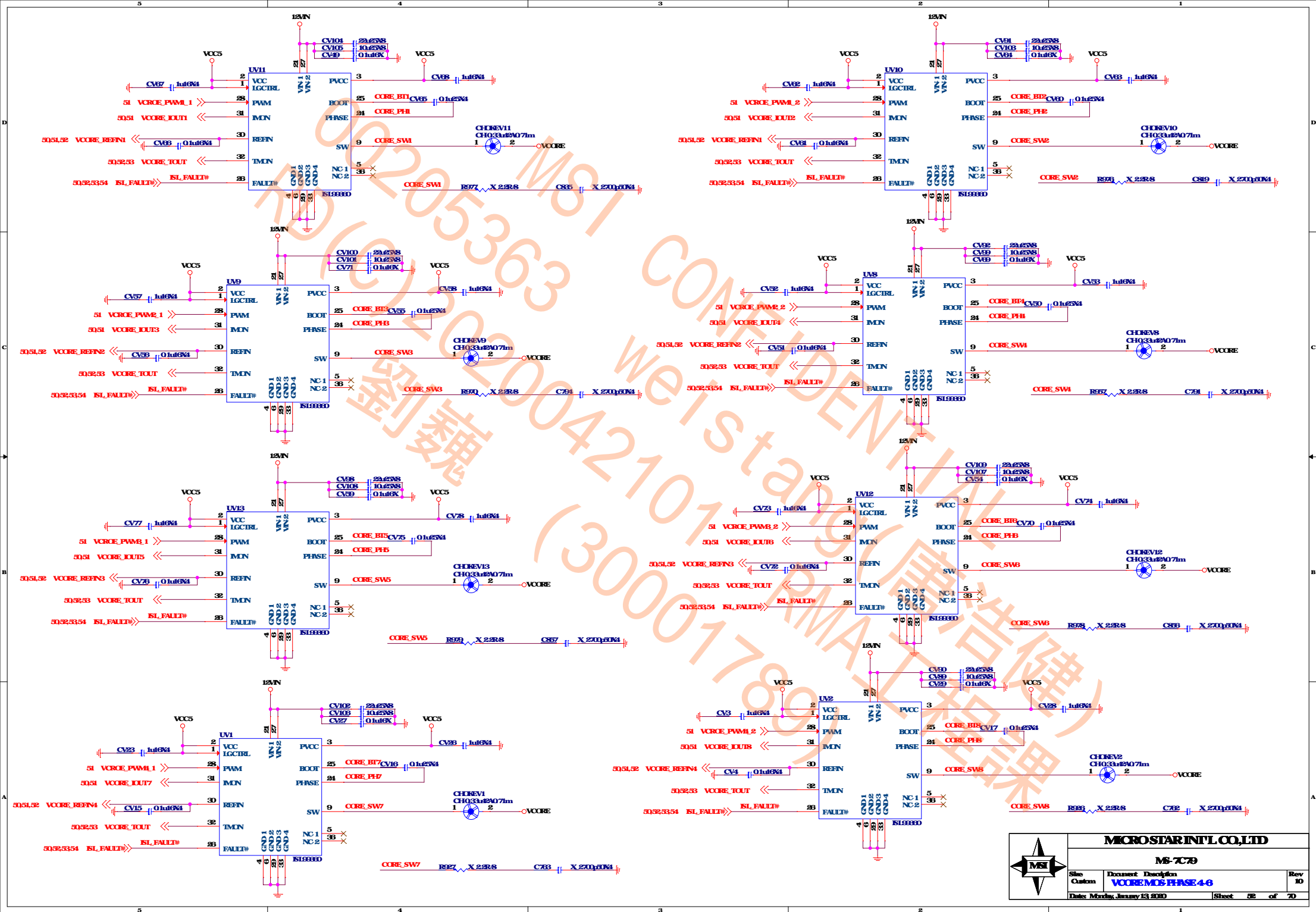
VCORE Dable

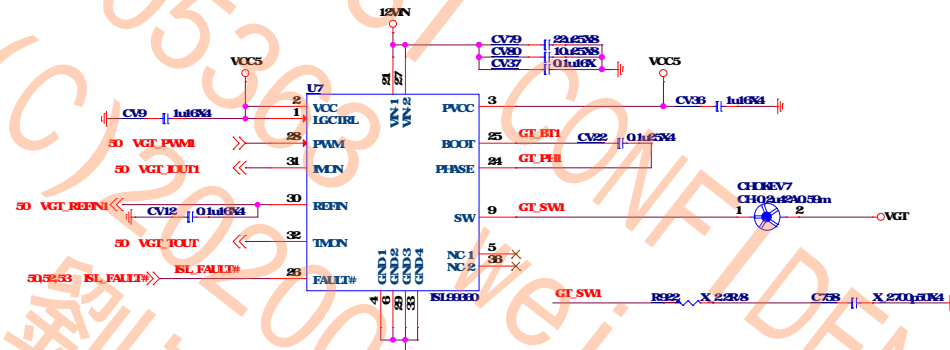
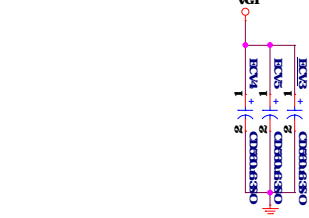


MICROSTAR INT'L CO., LTD

MS-7C79

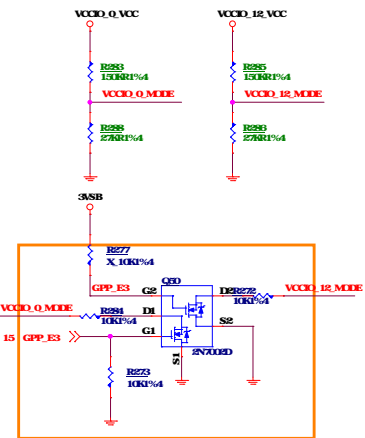
Site	Document Description	Rev
Custom	VCORE MOS PHASE 1-3	10
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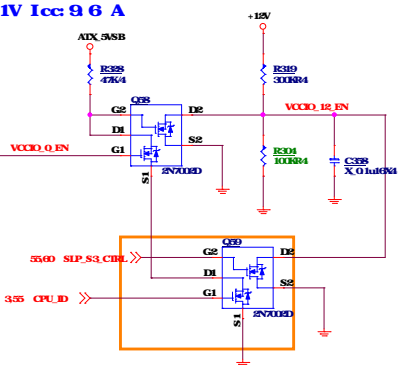
VCCIO 0 Power

0.95V Icc: 6.4 A
1.05V Icc: 8.3 A

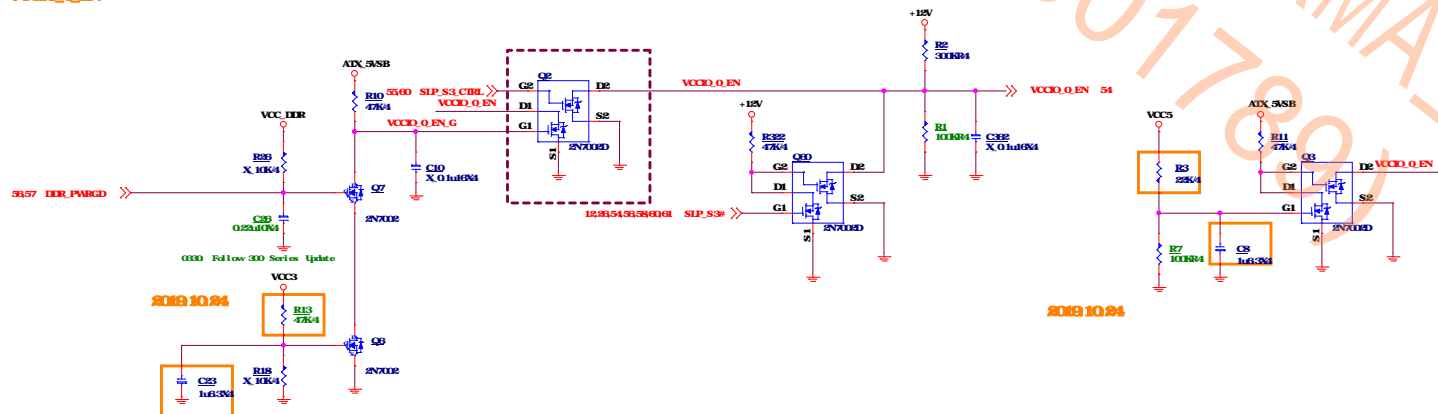


MODE:
(10%20%)*VCC > P0EM (Freq 500Hz)
(0-10%)*VCC > P0EM (Freq 500Hz)

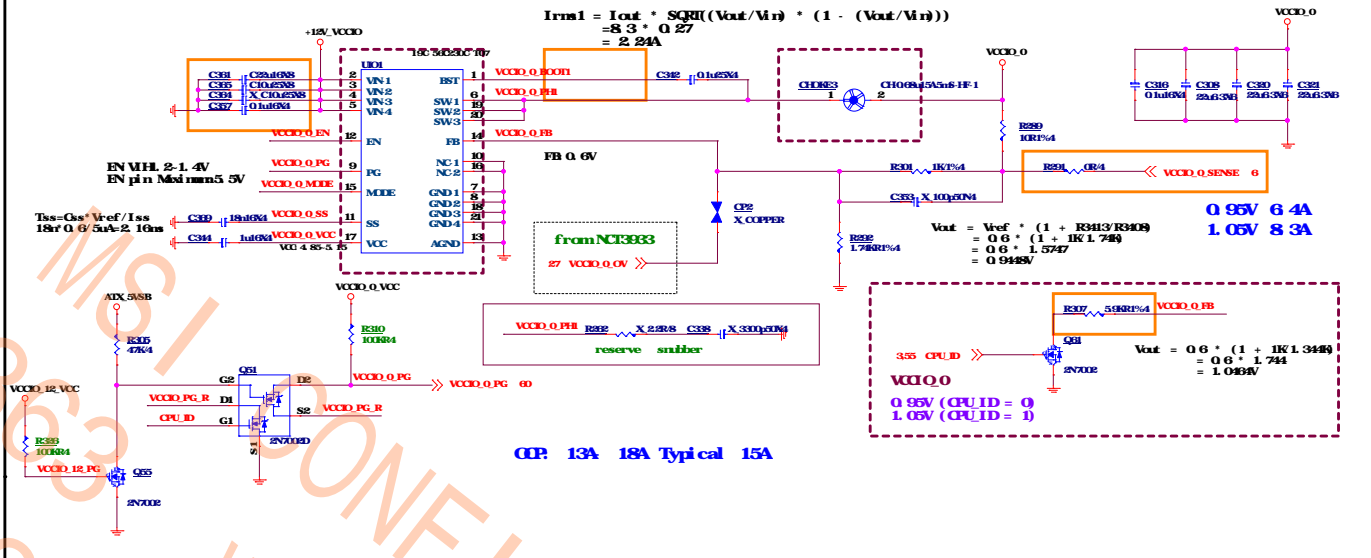
VCCIO_12_EN 1V Icc: 9.6 A



VCCIO_0_EN

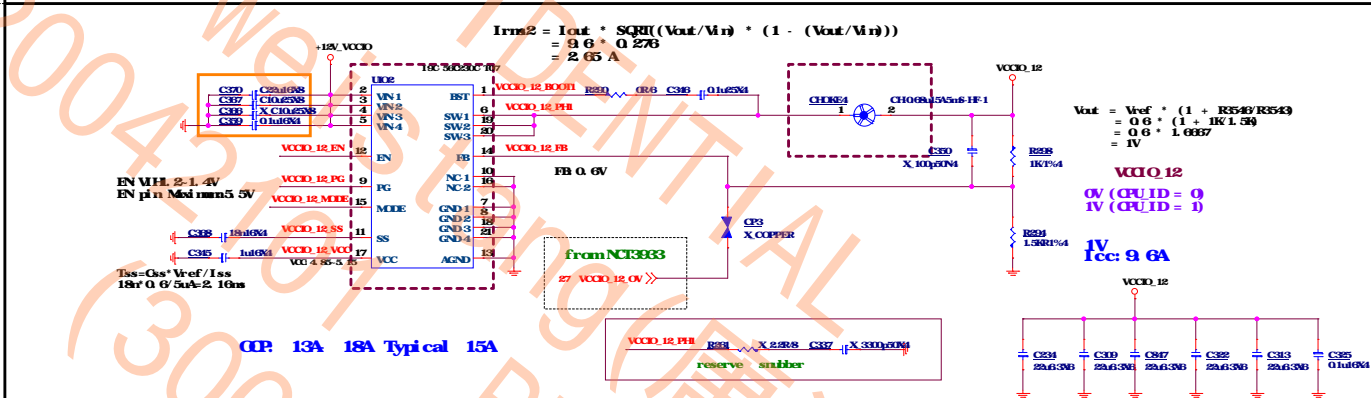


$$I_{rrm1} = I_{out} * \sqrt{R_{th}}((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))$$
$$= 8.3 * 0.27$$
$$= 2.24A$$



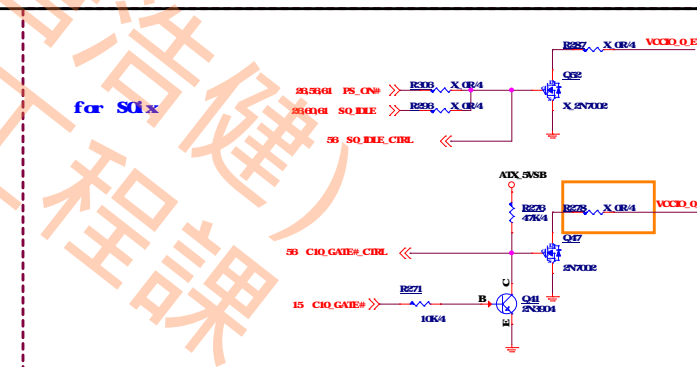
CCP: 13A 18A Typical 15A

$$I_{rrm2} = I_{out} * \sqrt{R_{th}}((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))$$
$$= 9.6 * 0.276$$
$$= 2.65A$$



CCP: 13A 18A Typical 15A

for S01x



DDR4 Power: 1.2V, 13.48A

3.68A For CPU
9.1A For DIMM
0.7A For DDR VTT

1.2V, ICC_max=14.1A

CCP Measure : 22A

IO3 402403 Q05 3 3-4 0min65V

CCP_max=Iocset*Rocset/Rison(nan)
=10uA*68k/3.3nA
=20.6A

CCP_min=Iocset*Rocset/Rison(max)
=10uA*68k/4nA
=17A

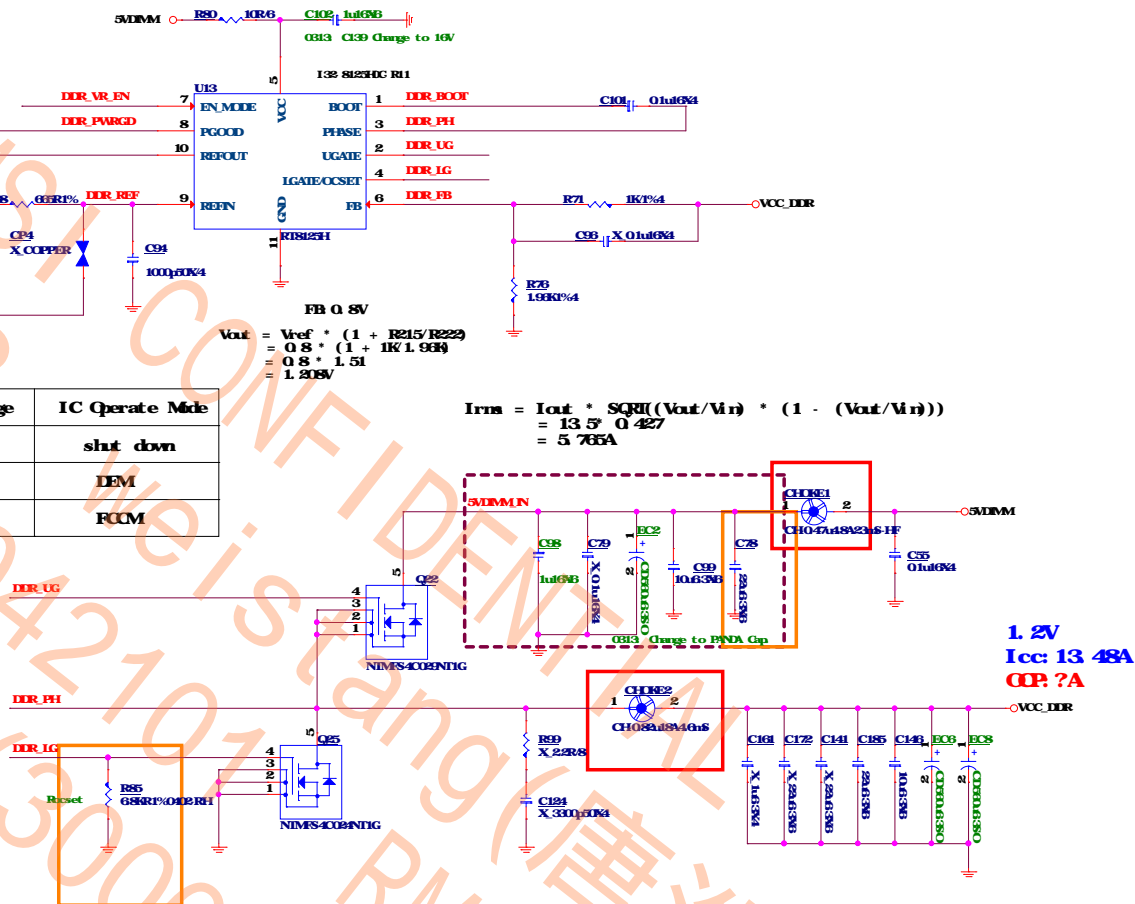
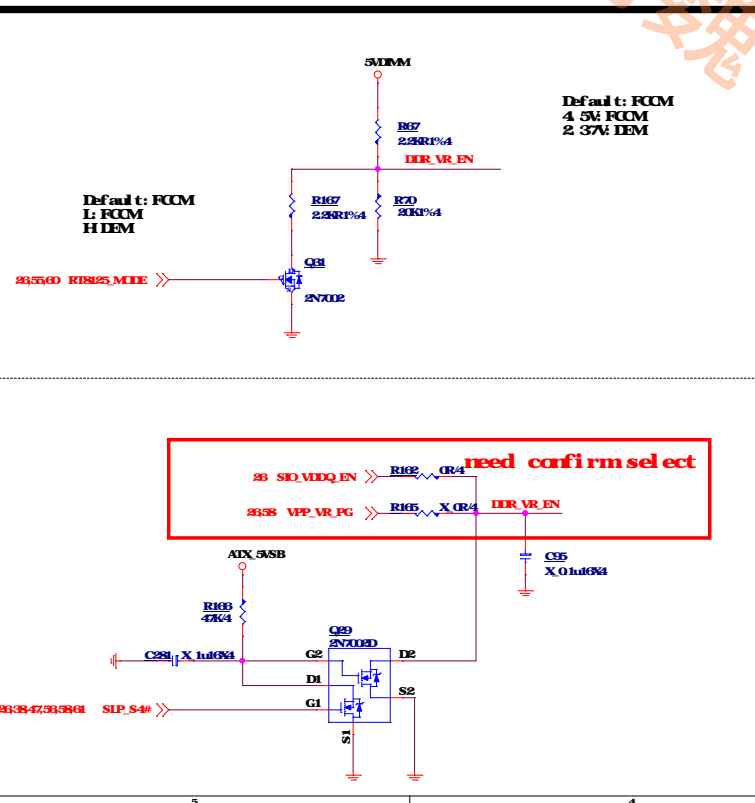
Output CHKE IO4 82B7080 M6 Isat=18A
I=20A L=0.6uH by L-I Curve

DDR_VR_EN
FROM SIO_VDDQ_EN R3438/R3441/R3439/Q38 stuff
FROM VPP_VR_PG R3438/R3441/R3439/Q38 un stuff

EN/MODE Pin Voltage	IC Operate Mode
<0.4V	shut down
2.1-2.7V	DEM
4.3-5V	FCOM

$$V_{out} = V_{ref} * (1 + R215/R222) \\ = 0.8 * (1 + 1K/1.93K) \\ = 0.8 * 1.51 \\ = 1.208V$$

$$I_{rms} = I_{out} * \sqrt{R_L((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))} \\ = 13.5 * 0.427 \\ = 5.765A$$



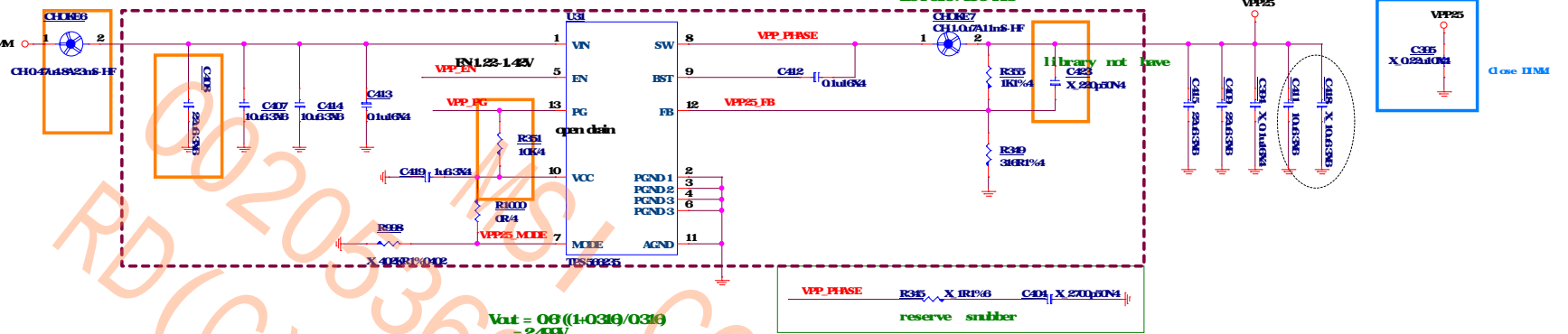
VPP2.5V Power: 2.5V, 6A (for dimm LED)

IC OCP: 7.6A (66A-86A)

$$I_{rms} = I_{out} * \sqrt{SQRT((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$

$$= 6 * 0.5$$

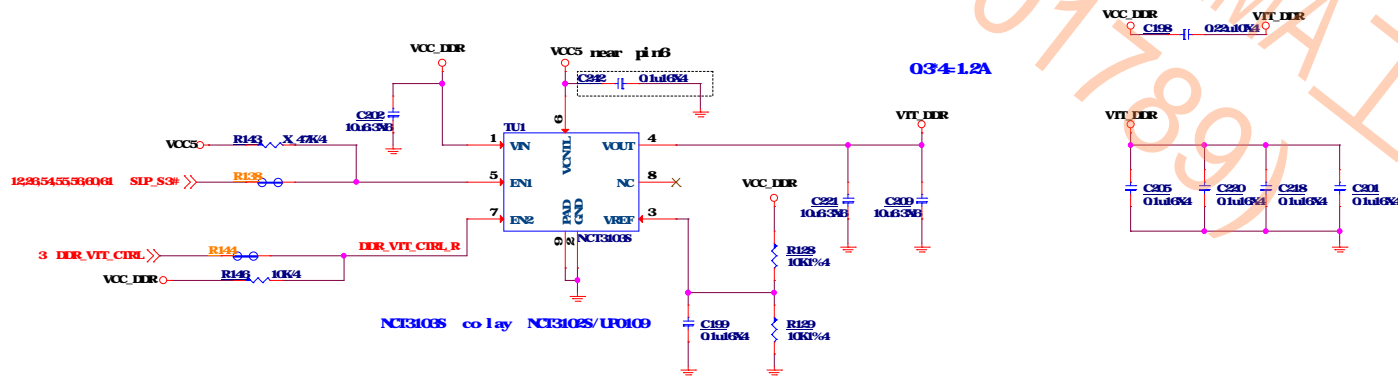
$$= 3A$$



Vmode(VPP25_MDE)	0-0.3V	0.3-1.2V	>1.2V
Rmode	OR	100K-150K	To VCC (recommand) or R-400K
Operating Mode	Eco Mode	Off-Of-Audio	ROOM

DDR VTT Power:

To CPU Copper trace width > 250mils, Fill island behind DIMM > 40mils.



PCH_IP05_VSB Power: 1.05V, 17.651A

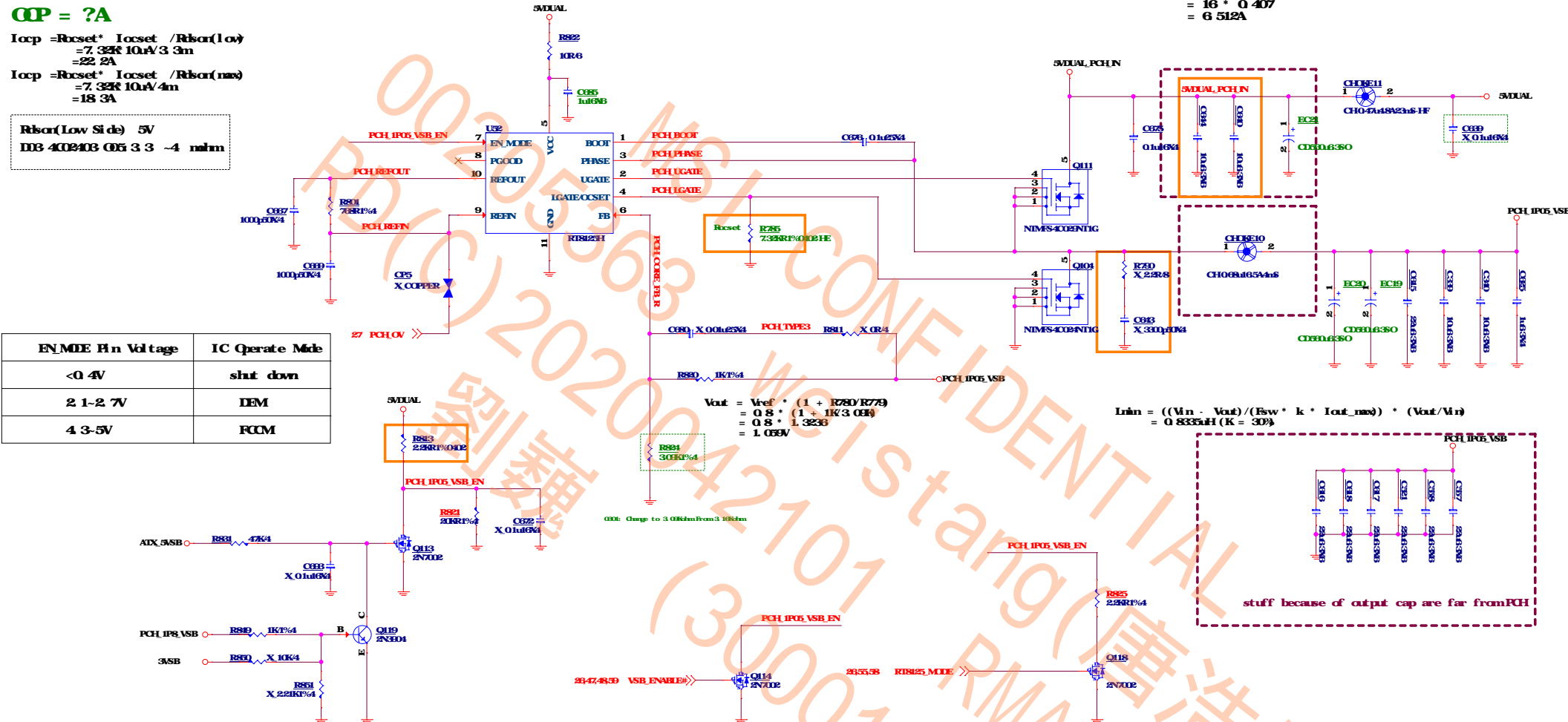
QCP = ?A

$$I_{cp} = R_{cset} \cdot I_{cset} / R_{sca}(low) = 7.32K \cdot 10uA / 3.3m = 22.2A$$

$$I_{cp} = R_{cset} \cdot I_{cset} / R_{sca}(nom) = 7.32K \cdot 10uA / 4m = 18.3A$$

R_{sca}(Low Side) 5V
D03 402403 05 3 3 -4 naim

EN/MOE Pin Voltage	IC Operate Mode
<0.4V	shut down
2.1-2.7V	DEM
4.3-5V	FCOM



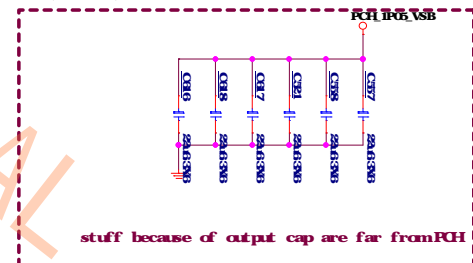
$$I_{rms} = I_{out} \cdot \sqrt{D \cdot (V_{out}/V_{in}) + (1 - D) \cdot (V_{out}/V_{in})^2}$$

$$= 16 \cdot \sqrt{0.407}$$

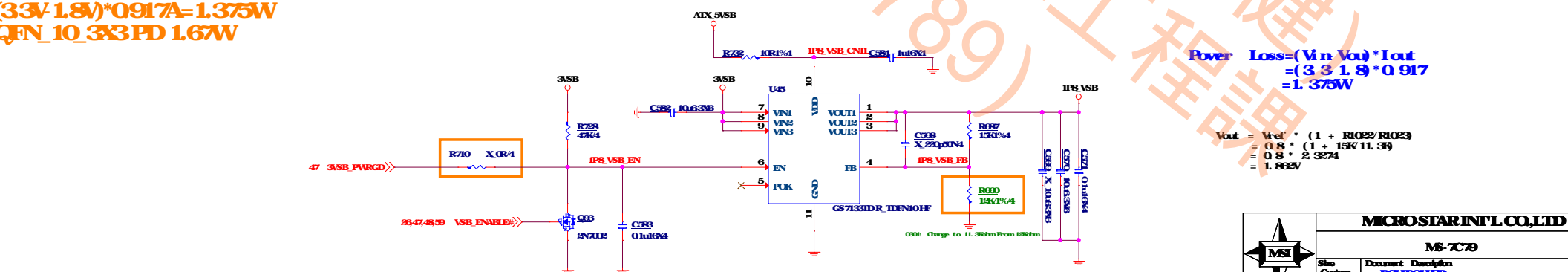
$$= 6.512A$$

$$I_{lim} = ((V_{in} - V_{out}) / (f_{sw} \cdot k \cdot I_{out_max})) \cdot (V_{out}/V_{in})$$

$$= 0.8335uH (K = 30)$$



IP8_VSB Power: 1.8V, 0.917A (3.3V-1.8V)*0.917A=1.375W QFN_10 3x3 PD 1.67W



$$Power\ Loss = (V_{in} - V_{out}) \cdot I_{out}$$

$$= (3.3 - 1.8) \cdot 0.917$$

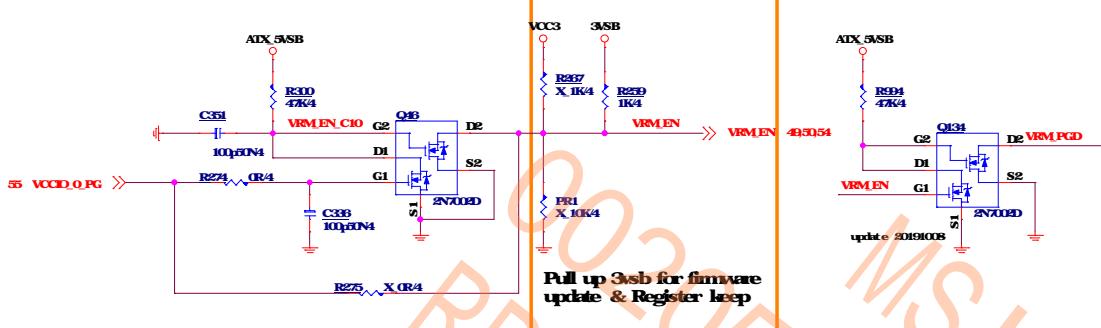
$$= 1.375W$$

$$V_{out} = V_{ref} \cdot (1 + R_{102}/R_{103})$$

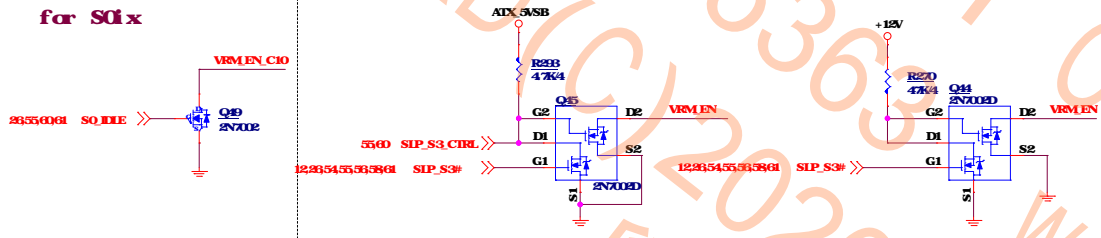
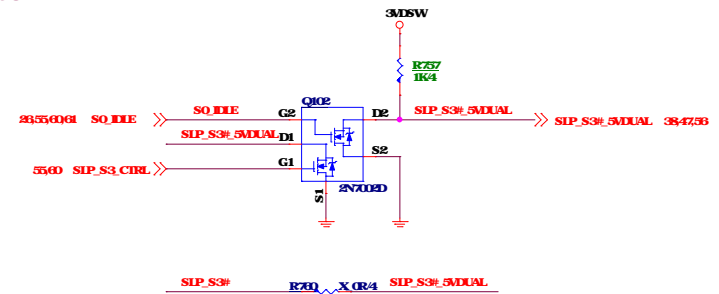
$$= 0.8 \cdot (1 + 15K/11.3K)$$

$$= 0.8 \cdot 2.3274$$

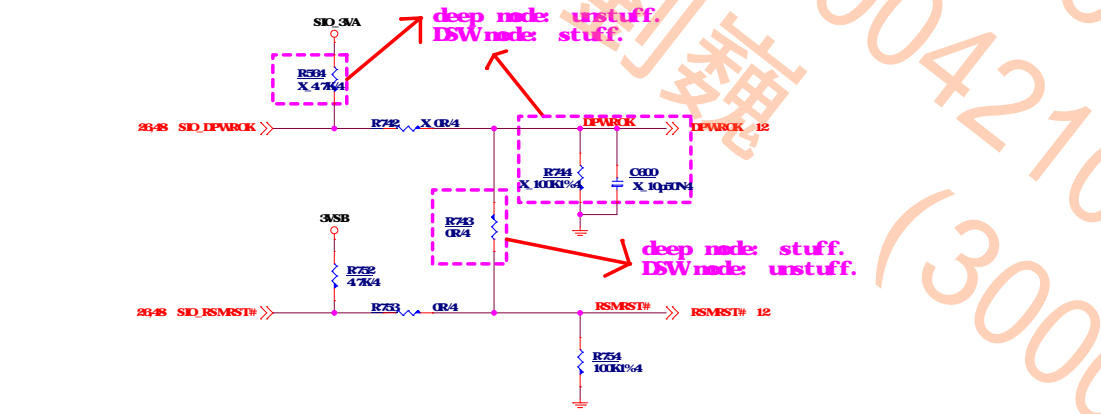
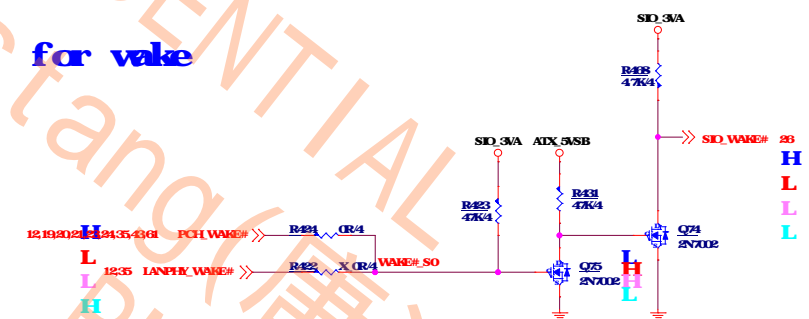
$$= 1.862V$$



for S01x

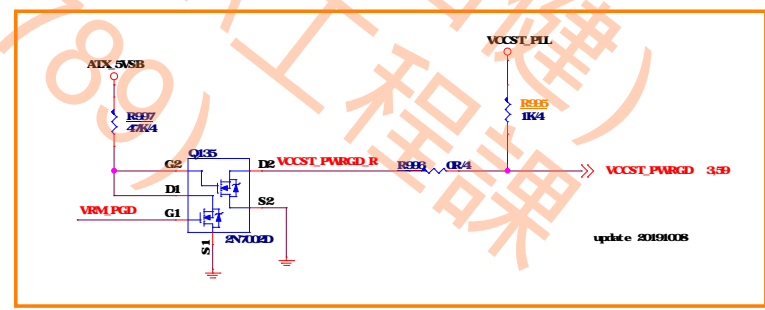
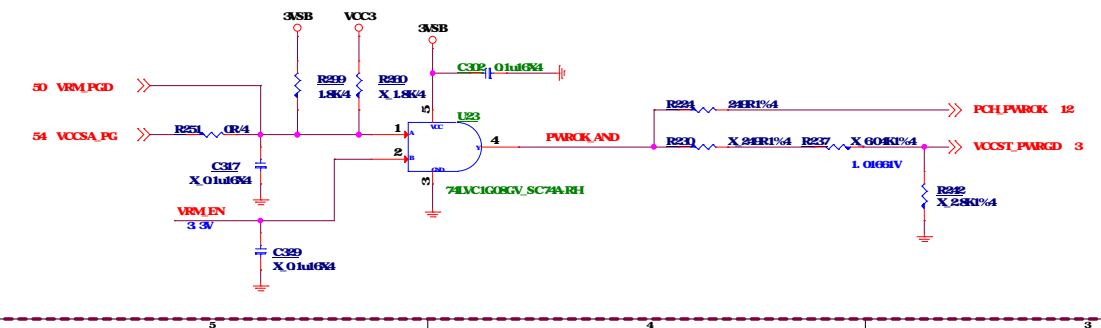


for wake

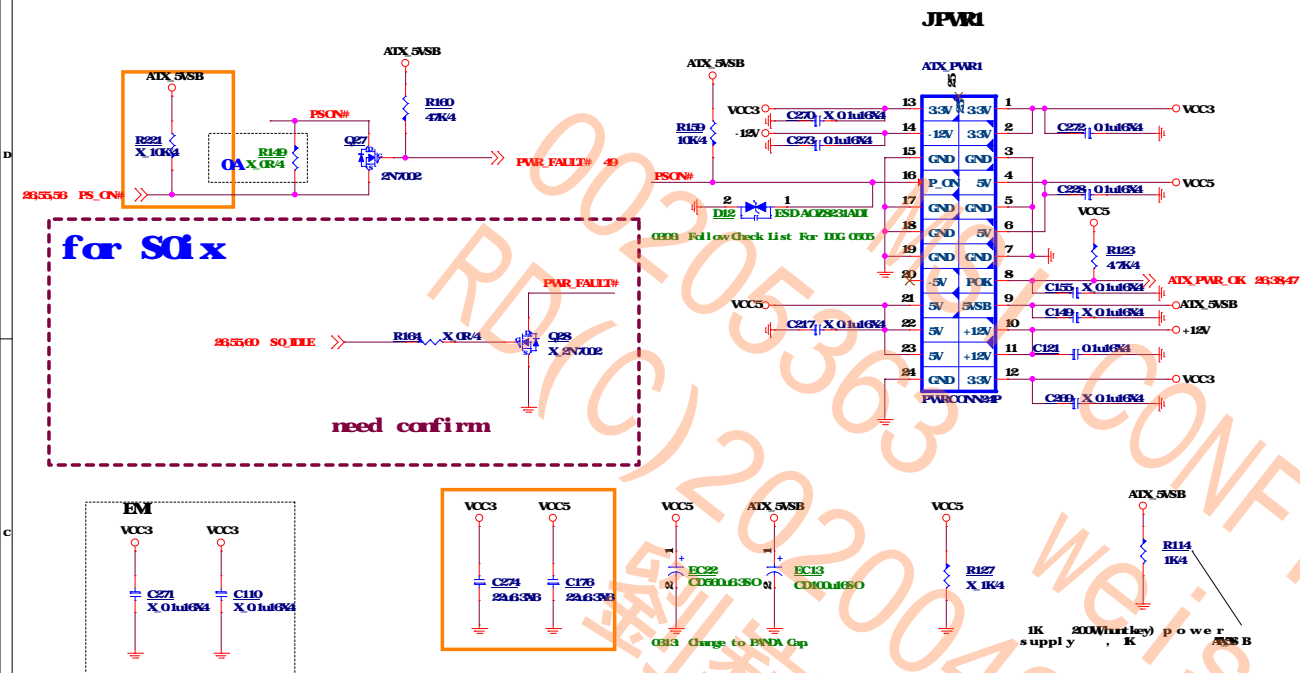


Notice Pwmic VRM_PG pin sink low capability!

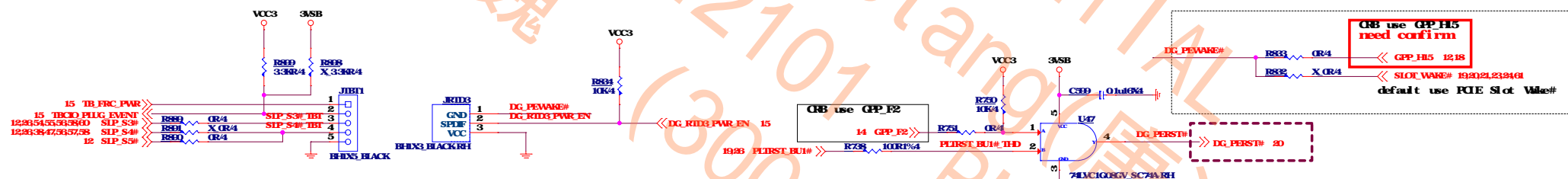
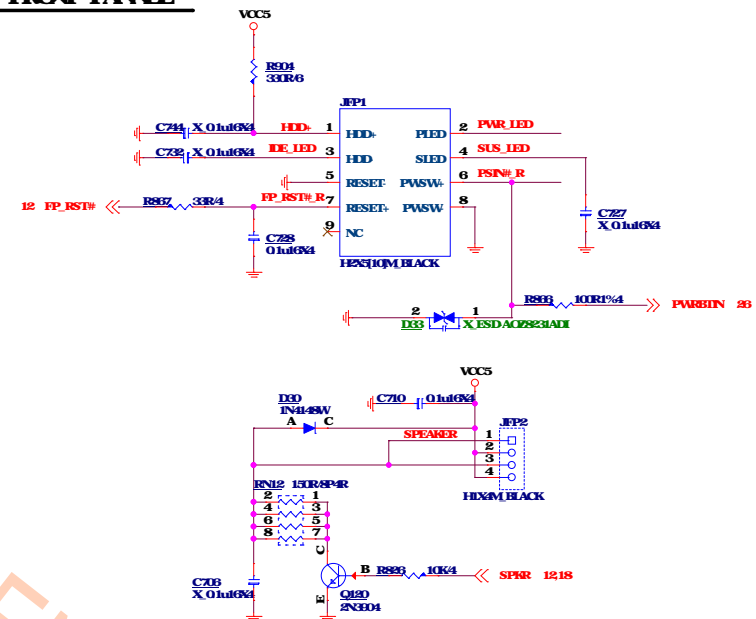
Main : T3901G0820N47
AVL: T707SZ080107
T707SZ0880005



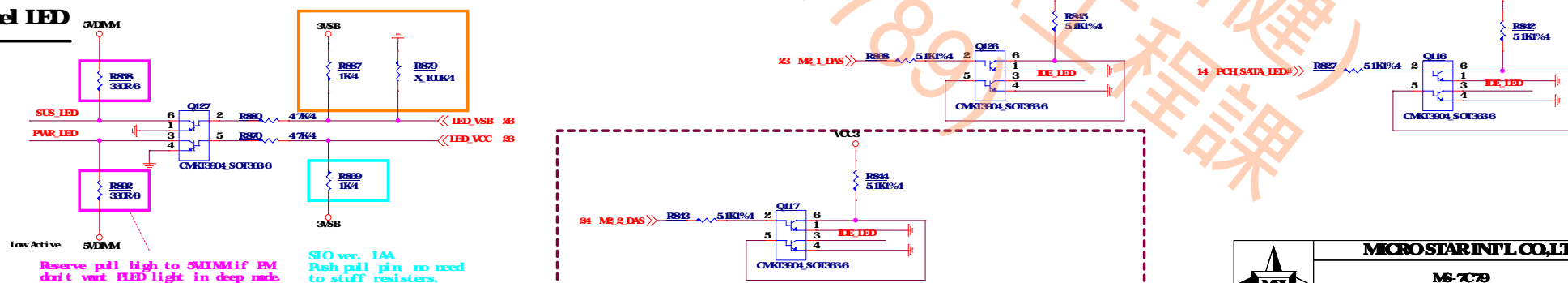
ATX POWER CONNECTOR



FRONT PANNEL



Front Panel LED



MICROSTAR INT'L CO., LTD

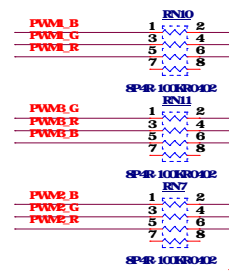
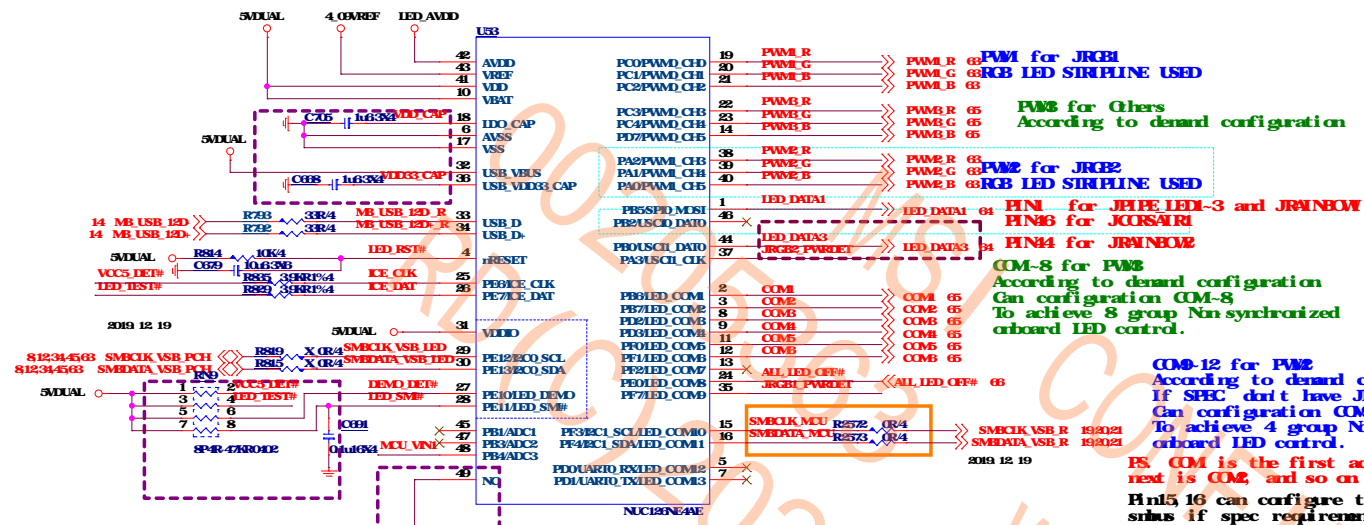
MS-7C79

Size Custom	Document Description ATXConnector_F_Panel
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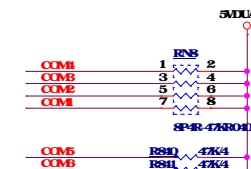
	Rev 10
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LED MCU



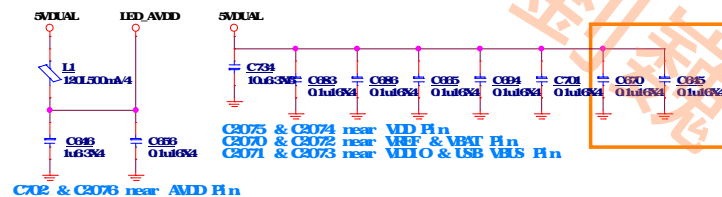
Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUTO Cover	LED_GPIO.01	No Use
MS/IO cover	LED_GPIO.02	No Use
JRAINBOW	LED_GPIO.03	No Use
JCOSAIRI	LED_DATA2	No Use
JRGB/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1-8	PWM3
Board Side LED	COM 9-16	PWM2



COM-12 for PWM2
According to demand configuration
If SPEC don't have JRGB2
Can configuration COM-12
To achieve 4 group Nn synchronized
onboard LED control.

PS. COM is the first action block,
next is COM2, and so on

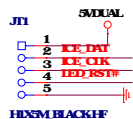
Hn15 16 can configure to master
sinus if spec requirement.



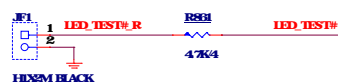
IF no JPVALED1 & JP1PE_LED spec

MCU can be powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

JT1 for FWupdate

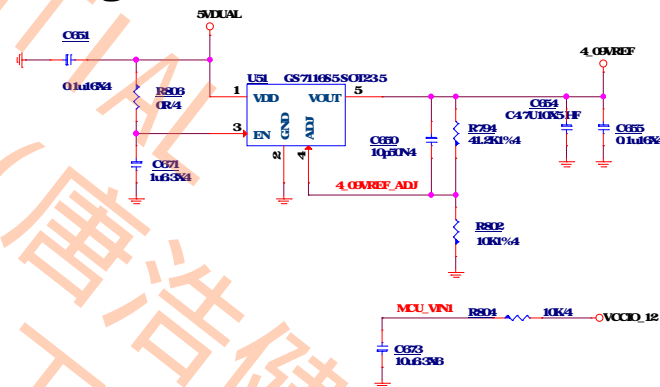


JF1 for Factory test



Check with LED model spec

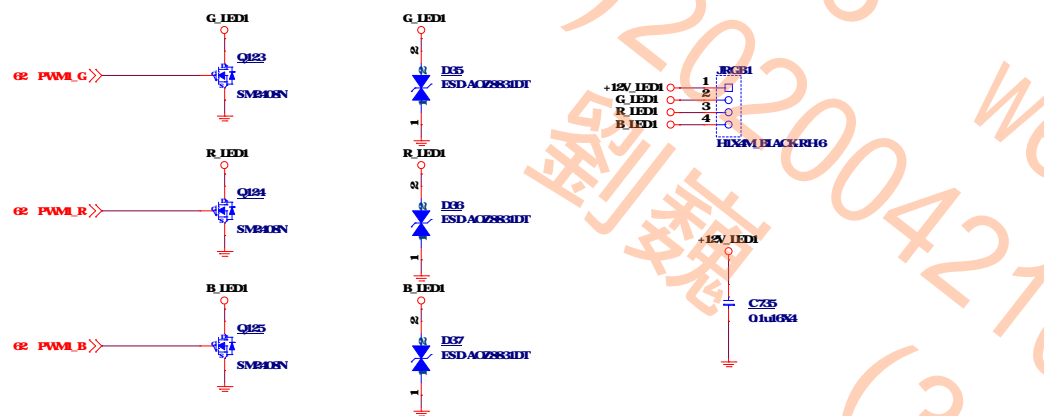
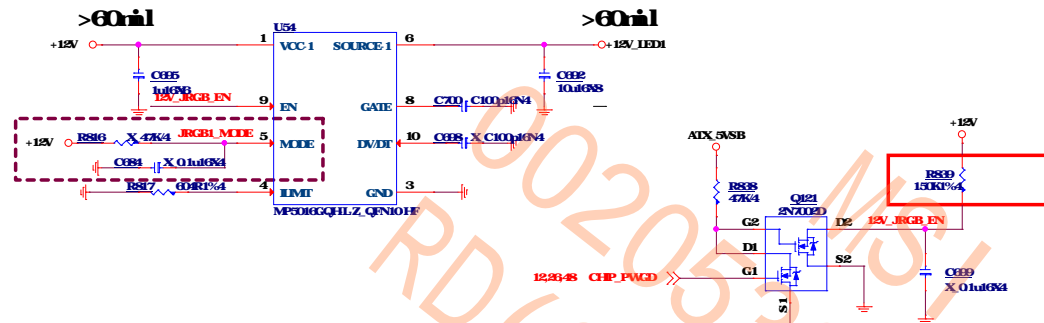
Voltage HW monitor



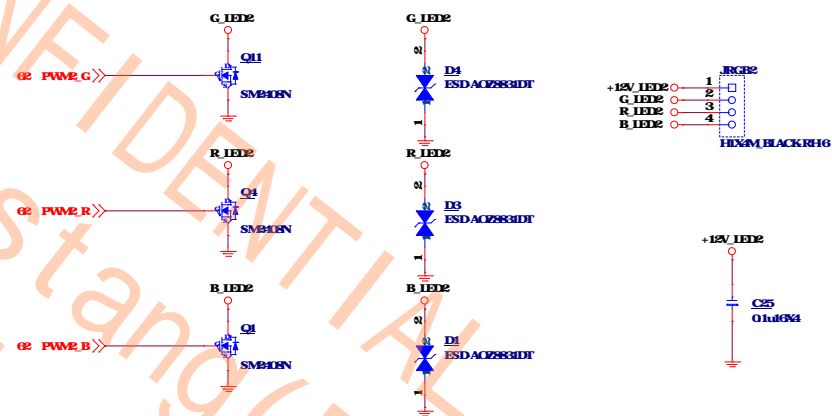
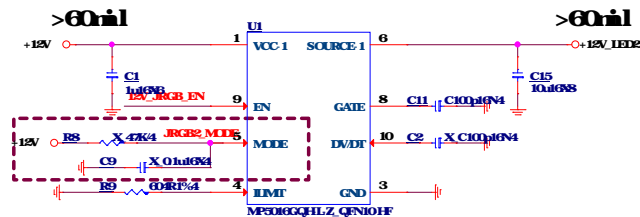
Option spec for voltage monitor require
VDD1, 2, 3 is example.

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MS-7C79			
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Custom	MCU Control	B0	
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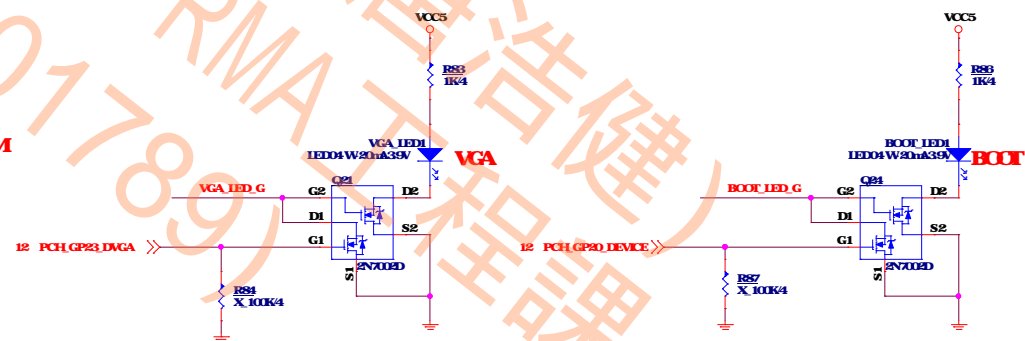
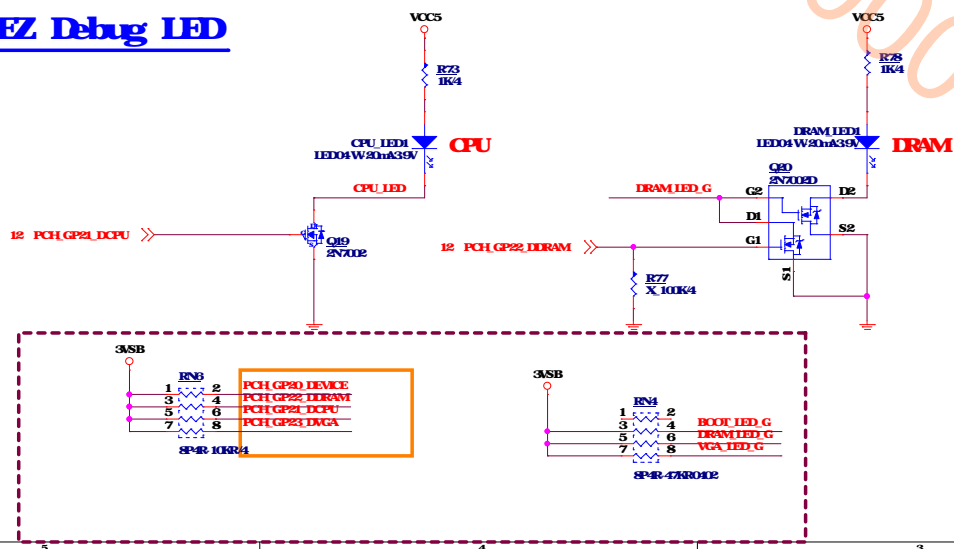
JRCB1



JRCB2



EZ Debug LED



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MS-7C79

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Custom	JRCB and EZ Debug LED	10000000
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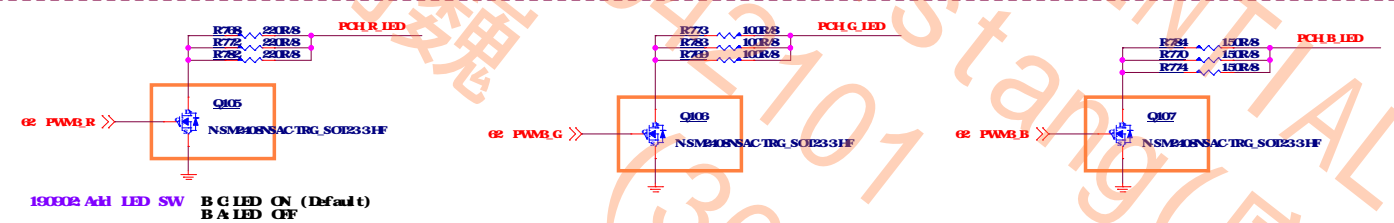
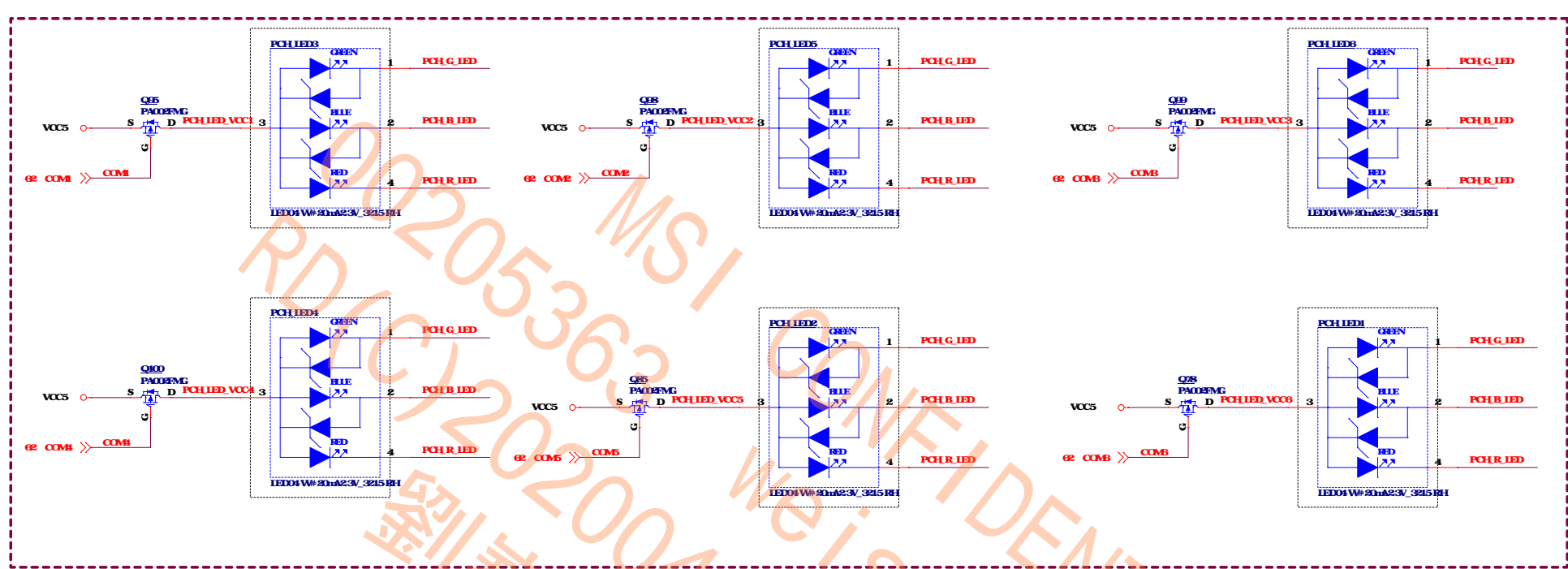
JRAINBOW1 LED



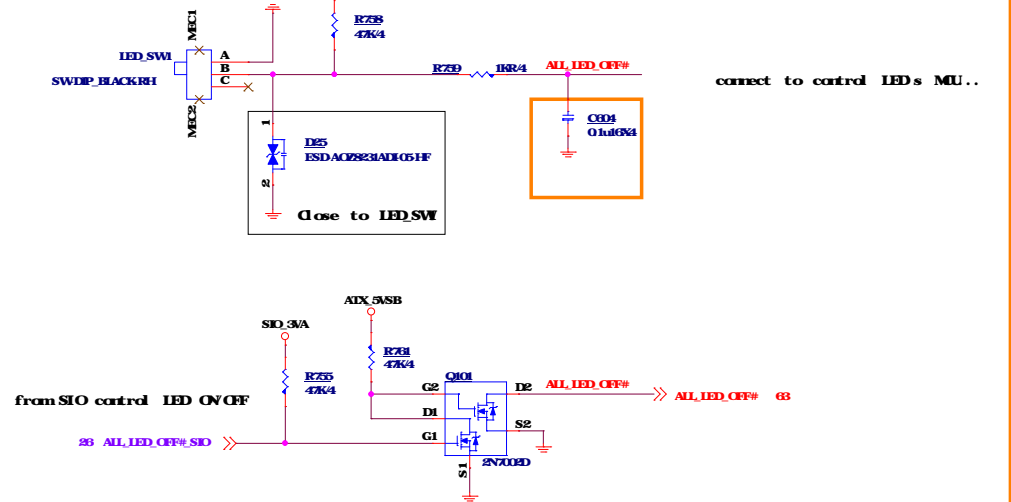
JRAINBOW2 LED



PCH_LED



LED_SWITCH



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MS-7C79			
Site	Document	Description	Rev
Custom		BOARD SIDE LED	
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7C70A



CPU_HI



BIOS_X1
BATDCR002P



HDMI LABEL



CFPS LABEL



NATIVE LABEL



BIOS LABEL

Heat Sink



OE37C7001A87



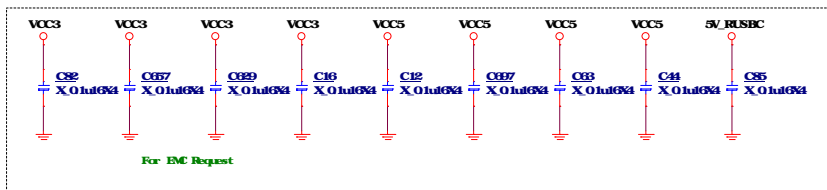
OE37C7001A87



OE37C7001A87

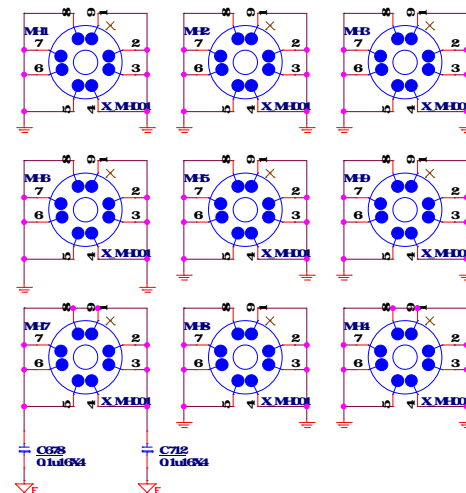


COVER_M2_HS1

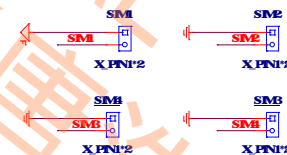


For EMC Request

Murting Hles



Simulation



Optical Fducia Marks 120

